frequency telemetry for which specific converters are available, most situations call for either an immediate analog presentation or an analog-to-digital conversion. In any case the detector must have an adequate input impedance—usually high because it is intended to measure the bridge output voltage—and an input arrangement compatible with ground connections in the bridge supply. In particular, the meter input must be differential if the bridge supply is grounded.

The easiest choice for an immediate analog presentation is a galvanometer. It is inherently differential, which is an advantage when compared with other detectors. But its input impedance is medium to low, and it lacks the necessary robustness for industrial applications if it must also be sensitive. Furthermore it is too slow for dynamic measurements, and in general it works only for dc supplies. Although galvanometers were the better choice before the advent of integrated circuits, these shortcomings reduce its application in present measurement systems.

An oscilloscope is an alternative to galvanometers when a dynamic signal is being measured. When no probe is used, it presents a 1-MΩ input resistance, which is high enough for most cases. But unless the bridge power supply is floating and the external interference is small, it must have a differential input. If a high sensitivity is also required, its cost can be very high. An alternative to oscilloscopes are paper and chart recorders, but both require the input signal to be amplified. Therefore we consider these to be presentation methods for amplified signals.

Whether for an immediate digital presentation or for digital transmission or calculation, the analog bridge output signal must be converted into digital form. If a bench or panel voltmeter is used, that function is performed by the instrument, which has an input resistance of 10 MΩ or higher. But because of its cost and lack of flexibility, the use of such a subsystem is not always the best solution. Nevertheless, there is an increasing availability of custom-tailored digital panel meters that also offer a simultaneous digital output signal for remote connection.

Amplification techniques suitable to convert low-amplitude bridge signals into 1 or 10 V signals, as required by usual ADCs at their inputs, are dealt with in the next section.

## 3.5 INSTRUMENTATION AMPLIFIERS

### 3.5.1 Differential Amplifiers

Most resistance sensor bridges are supplied by a grounded voltage or current source. Therefore the amplifier at the bridge's output should not have any of its input terminals grounded. In addition we will show later that it is best for input terminals to have high and similar impedances to ground. An amplifier having these characteristics is called a *differential amplifier*.

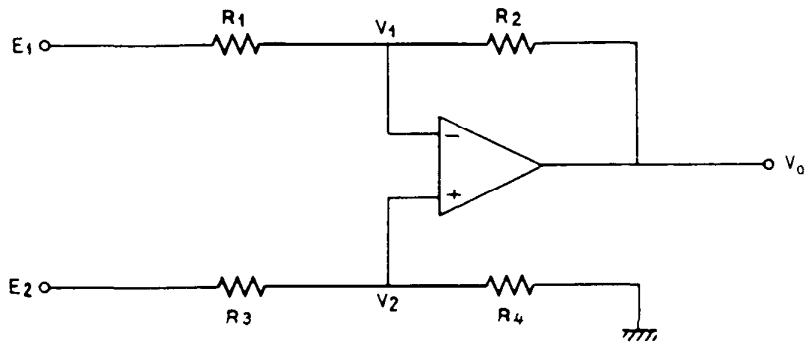


**FIGURE 3.36** Differential amplifier based on a single op amp.

Figure 3.36 shows a very simple circuit to implement a differential amplifier. We assume that the op amp is ideal ($V_1 = V_2$); then the output voltage is

$$V_o = -\frac{R_2}{R_1} E_1 + \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3 + R_4} E_2 \tag{3.47}$$

To illustrate the differential properties of the circuit, it is convenient to write the output as a function of the differential input voltage $E_d = E_2 - E_1$. In order to do this, we must make the following substitutions in (3.47)

$$E_d = E_2 - E_1 \tag{3.48}$$

$$E_c = \frac{E_1 + E_2}{2} \tag{3.49}$$

where $E_c$ is the common mode voltage. Substitution of (3.48) and (3.49) in (3.47) yields an equation where there is one factor multiplying $E_c$ and another multiplying $E_d$. The first factor is called *common mode gain*, $G_c$, and the second factor *differential mode gain*, $G_d$. That is,

$$V_o = G_c E_c + G_d E_d \tag{3.50}$$

Their expressions for the circuit in Figure 3.36 are

$$G_c = \left.\frac{V_o}{E_c}\right|_{E_d=0} = \frac{R_4 R_1 - R_2 R_3}{R_1(R_3 + R_4)} \tag{3.51}$$

$$G_d = \left.\frac{V_o}{E_d}\right|_{E_c=0} = \frac{1}{2}\left[\frac{R_2}{R_1} + \left(1 + \frac{R_2}{R_1}\right)\frac{R_4}{R_3 + R_4}\right] \tag{3.52}$$

In a differential amplifier we wish to amplify the difference between the input voltages but not the common mode signal. Thus we must have $G_c = 0$, which is obtained when

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} = k \tag{3.53}$$

Then $V_o = kE_d$. Because the matching expressed by (3.53) is difficult to fulfill exactly, the circuit's ability to reject common mode signals will be limited rather than infinite. It is quantified by means of the Common Mode Rejection Ratio (CMRR), defined as the differential gain divided by the common mode gain. For Figure 3.36 it is given by

$$\text{CMRR} = \frac{G_d}{G_c} = \frac{1}{2}\,\frac{R_1R_4 + R_2R_3 + 2R_2R_4}{R_1R_4 - R_2R_3} \tag{3.54}$$

The CMRR is usually expressed in decibels. We obtain that by taking the decimal logarithm of the previous expression and multiplying the result by 20.

If in Figure 3.36 the op amp is not ideal we must substitute the model in Figure 3.37, where the common mode gain for the op amp ($A_c$) is obtained from the CMRR in the specification sheets. For the $\mu$A 741, for example, $A_d$ = 50,000 minimum at dc, and CMRR = 70 dB minimum. Therefore

$$A_c = \frac{A_d}{10^{70/20}} = 15.8$$

Using this model for the op amp, the analysis of Figure 3.36 is more cumbersome. But we can follow the same steps that lead us before to equations (3.47–3.50), now defining $V_d$ and $V_c$ from $V_1$ and $V_2$. Fortunately, after simplifying and reordering, from the final equation we obtain a very simple rule,

$$\frac{1}{\text{CMRR}_{\text{TOTAL}}} = \frac{1}{\text{CMRR}_{\text{R}}} + \frac{1}{\text{CMRR}_{\text{OA}}} \tag{3.55}$$

That is, the CMRR for resistors, equation (3.54), and for the op amp add in "parallel"; that is, their reciprocals add. Each CMRR must be expressed as a fraction, not in decibels.

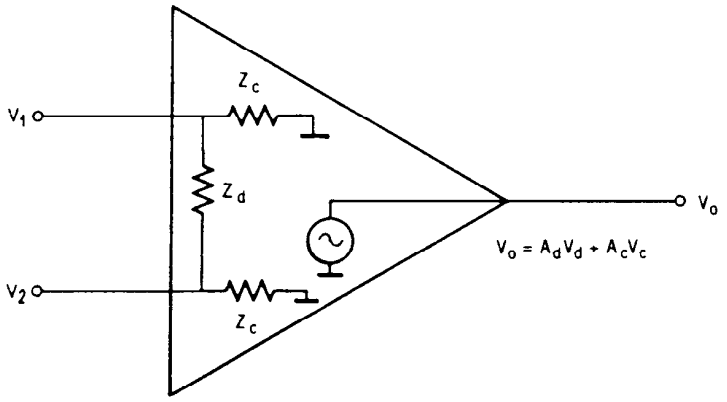


**FIGURE 3.37** Model describing the differential circuit of a real op amp.

The circuit of Figure 3.36 can be directly applied to a sensor bridge, where $E_1$ and $E_2$ are the voltages at the bridge output terminals. It is also possible to arrange connections in order to identify output bridge voltages with $V_1$ and $V_2$, as shown in Figure 3.38*a*.

For Figure 3.36, note that by assuming an ideal op amp, the input impedances seen by sources $E_1$ and $E_2$ are respectively $R_1$ and $R_3 + R_4$, implying that $R_2$ and $R_4$ will have to be very large resistors if high input impedance and high gain are required. A high input impedance is required in order to reduce loading effects in voltage measurements. The requirement for a high gain is due to the low amplitude for the bridge output. It would certainly be possible to arrange several gain stages in cascade in order to obtain the amplitude needed at the ADC input, but drifts and noise effects in amplifiers are lower when the gain is concentrated in the first amplifying stages (see Chapter 7). Figure 3.38*b* shows the equivalent circuit for analyzing Figure 3.38*a*. If, as usual, we want to have $V_0 = 0$ when $x = 0$, then we must have $R_2 = R_4 (= R)$. By applying (3.54), we obtain

$$\text{CMRR} = \frac{1}{2}\frac{1/2 + [(1 - x)/(2 + x)] + (2R/R_0)}{x/[2(2 + x)]} \tag{3.56}$$

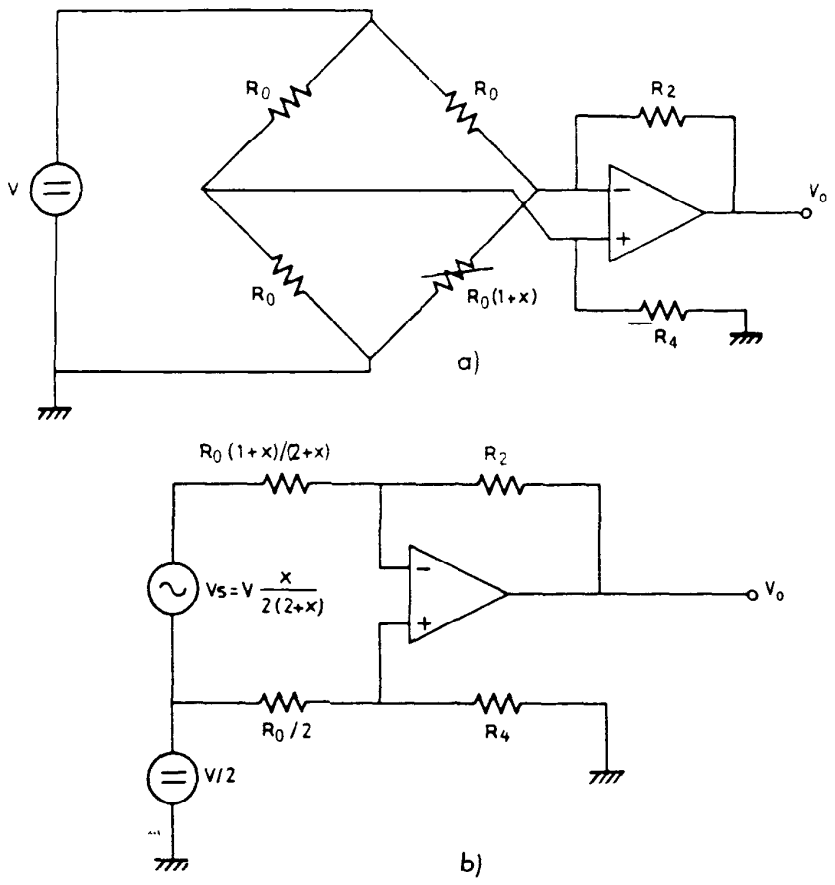


**FIGURE 3.38** Differential amplifier connected to a sensor bridge and its equivalent circuit.

For the case $x \ll 1$,

$$\text{CMRR} \cong \frac{1 + 2R/R_0}{x/2} \tag{3.57}$$

Thus the CMRR for this circuit degrades when the bridge imbalance increases. If, for example, we want a differential mode gain of 100 when $x = 0.01$, the resulting CMRR will be approximately 86 dB. Therefore the actual common mode gain, $G_c$, is about $5 \times 10^{-3}$. If the supply voltage for the bridge is 20 V, then the common mode voltage at the bridge output will be $20/2 = 10$ V. The voltage contribution at the amplifier output will be 50 mV on a signal voltage of 5 V, even with an ideal op amp. This contribution is proportional to $x$, so the result is a small change in gain. For large values of $x$ the nonlinearity is increased.

Both the circuit in Figure 3.38*a* and that in Figure 3.36 show the additional shortcoming of the need for modifying two resistors whenever the differential mode gain is to be changed. Even more, this modification must be performed without degrading the matching required by equation (3.57). This lack of flexibility has lead to the development of better alternatives, implemented in circuits generally called instrumentation amplifiers.

### 3.5.2 Instrumentation Amplifiers Based on Two op Amps

An *instrumentation amplifier* is an electronic circuit that simultaneously yields: high input impedance; high common mode rejection; high stable gain that can be adjusted by a single resistor and without a trade-off between gain and bandwidth (as happens in op amps); low value and low drift for offset voltage and currents; and low output impedance. Commercially available units exhibiting these performances are in the form of monolithic, hybrid, or modular ICs. Hybrid and modular models are based on two basic topologies called "two-op-amp instrumentation amplifier" and "three-op-amp instrumentation amplifier."

The analysis of these basic circuits is of great interest because they can be implemented by using inexpensive discrete components. The performance is adequate for many applications and can sometimes be built quicker and at lower cost than when using integrated units.

Figure 3.39 shows the basic structure for a two-op-amp-based instrumentation amplifier. We consider the op amps ideal, then repeat the same steps leading to (3.47–3.50). Then the necessary condition to obtain an infinite CMRR is also that expressed by (3.53). The output voltage is then

$$V_o = E_d \left(1 + k + \frac{R_2 + R_4}{R_g}\right) \tag{3.58}$$

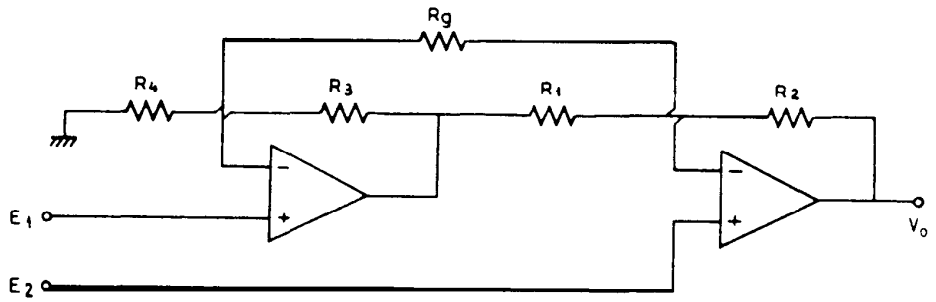


**FIGURE 3.39** Instrumentation amplifier based on two op amps.

Therefore, although it is also necessary to match four resistors, now by means of $R_g$ it is possible to change the gain without affecting the matching of those four critical resistors. A shortcoming of this circuit is the possible saturation of the first op amp when the common mode input signal is large. To avoid that saturation, the following condition must be fulfilled:

$$\left(|E_c| + \left|\frac{E_d}{2}\right|\right)\left(1 + \frac{R_3}{R_4}\right) < V_{\text{saturation}} \tag{3.59}$$

### 3.5.3 Instrumentation Amplifiers Based on Three op Amps

The circuit in Figure 3.40 is the classic implementation for an instrumentation amplifier. Its analysis when the three op amps are ideal leads to

$$\frac{V_A - E_1}{R_1} = \frac{E_1 - E_2}{R_2} = \frac{E_2 - V_B}{R_3} \tag{3.60}$$

$$\frac{V_B - V_C}{R_6} = \frac{V_C}{R_7} \tag{3.61}$$

$$\frac{V_A - V_C}{R_4} = \frac{V_C - V_o}{R_5} \tag{3.62}$$

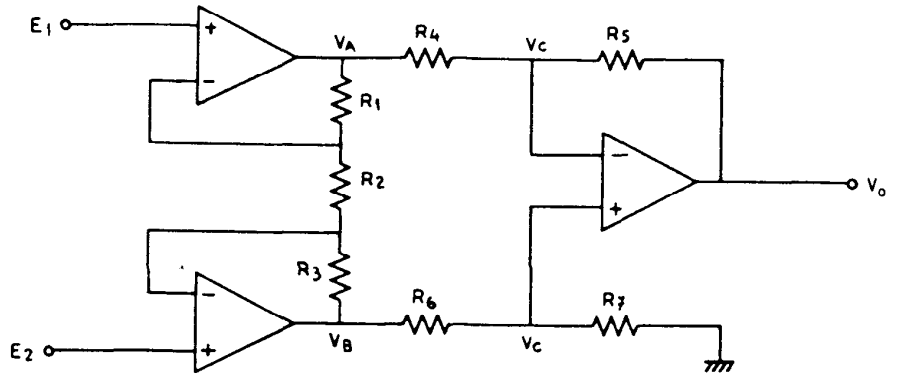


**FIGURE 3.40** Instrumentation amplifier based on three op amps.

By eliminating $V_A$, $V_B$, and $V_C$ in the preceding equations, we have

$$V_o = -E_1\left(\frac{R_3}{R_2}\frac{R_7}{R_7+R_6}\frac{R_4+R_5}{R_4}+\frac{R_1+R_2}{R_2}\frac{R_5}{R_4}\right) + E_2\left(\frac{R_7}{R_2}\frac{R_2+R_3}{R_7+R_6}\frac{R_4+R_5}{R_4}+\frac{R_1}{R_2}\frac{R_5}{R_4}\right) \tag{3.63}$$

If again we consider the input differential mode and common mode signals. equations (3.48) and (3.49), the preceding expression leads to

$$V_o = -E_d\left[\frac{1+R_5/R_4}{1+R_6/R_7}\left(\frac{R_3}{R_2}+\frac{1}{2}\right)+\frac{R_5}{R_4}\left(\frac{1}{2}+\frac{R_1}{R_2}\right)\right] + E_c\left[\frac{1-R_6R_5/R_7R_4}{1+R_6/R_7}\right] \tag{3.64}$$

From this we find that the common mode rejection is maximal when

$$\frac{R_5}{R_4}=\frac{R_7}{R_6}=k \tag{3.65}$$

If in addition $2R_1/R_2 = 2R_3/R_2 = G$, then we have

$$G_d = k(1+G) \tag{3.66}$$

This shows that we can change the differential mode gain by means of $R_2$ (although not in a linear way) without affecting the CMRR.

The condition to prevent saturation in any of the first stage op amps is different from that found in two-op-amp instrumentation amplifiers. From the corresponding expressions for $V_A$ and $V_B$, we can deduce that the common mode input signal is amplified by 1 in the first stage:

$$V_A = -\frac{E_d}{2}(1+G)+E_c \tag{3.67}$$

$$V_B = +\frac{E_d}{2}(1+G)+E_c \tag{3.68}$$

Therefore $E_c$ can be higher than in two-op-amp instrumentation amplifiers, provided that $V_A$ and $V_B$ are kept below the saturation level for op amps.

In practice we have neither perfect resistor matching nor ideal op amps. This does not have any serious repercussions on input impedances that always reach very high values both in common mode and differential mode. The common mode rejection, however, is affected by matching of resistors in the differential input to single ended stage (the second one), matching of

input op amps, and by CMRR of the op amp in the second stage. It can be shown that in a similar way to that expressed by (3.55), all these factors combine by adding their reciprocals [8]:

$$\frac{1}{\text{CMRR}_{\text{TOTAL}}} = -\frac{1}{\text{CMRR}_1} + \frac{1}{\text{CMRR}_2} + \frac{1}{G+1}\left(\frac{1}{\text{CMRR}_3} + \frac{1}{\text{CMRR}_R}\right) \tag{3.69}$$

Subscripts 1 and 2 refer to input op amps and subscript 3 to that in the second stage. Resistor imbalance is quantified by

$$\text{CMRR}_R = \frac{1}{2}\frac{R_4R_7 + R_5R_6 + 2R_5R_7}{R_4R_7 - R_5R_6} \tag{3.70}$$

From (3.69) it follows that it is advisable to use a dual op amp at the input stage instead of two individual units because that will increase the chances of having $\text{CMRR}_1 = \text{CMRR}_2$, thus increasing the total CMRR.

The effect of tolerances in resistors can be analyzed from (3.70). If a tolerance $\alpha$ is assumed for all resistors, the worst-case condition would be when the denominator in (3.70) is maximal, corresponding to the situation $R_4 = R(1+\alpha)$, $R_7 = kR(1+\alpha)$, $R_5 = kR(1-\alpha)$, $R_6 = R(1-\alpha)$. The result is then

$$\text{CMRR}_R = \frac{1}{2}\frac{2 + 2\alpha^2 + 2k(1-\alpha^2)}{4\alpha} \tag{3.71}$$

and when $\alpha \ll 1$,

$$\text{CMRR}_R \approx \frac{k+1}{4\alpha} \tag{3.72}$$

**Example:** If we desire a differential mode gain of 1000 and use 5% tolerance resistors, how do the values for $G$ and $k$ influence the maximal CMRR that can be achieved? From (3.66),

$$1000 = k(G+1)$$

If the three op amps are considered to be ideal, from (3.69) and (3.72) it follows that

$$\text{CMRR}_{\text{TOTAL}} = \frac{(G+1)(k+1)}{4\alpha} \tag{3.73}$$

Therefore $\text{CMRR}_{\text{TOTAL}} = 1000(k+1)/0.2k = 5000(k+1)/k$. When $k = 1$, we achieve 80 dB; when $k = 10$, we achieve about 74 dB. It is thus better to

design a high gain for the first stage, unless other factors (drifts, noise) suggest low gain.

To avoid the need for low tolerance resistors, whenever a high CMRR is of interest, one of the four resistors in the differential stage (usually $R_7$) is an adjustable one. Another option is to use a second stage that already includes the entire differential stage, namely, the op amp and the resistors. That is the case, for example, with Burr-Brown Corp. models INA 105, INA 117, and 3627. These components can also be used in different applications, whether differential or not, because they make accessible one terminal of each internal resistor [9].

When the circuit in Figure 3.40 is built from discrete parts, we should consider the following. Bipolar input op amps are usually more linear and have lower offset voltage and drifts than FET input op amps. However, FET input op amps have lower bias currents and higher input impedances. In any case it is important for these two op amps to be matched in CMRR, equation (3.69) and in offset voltage. The need for offset voltage matching can be justified from (3.67) and (3.68) if they are rewritten when the offset voltage for each op amp is taken into account. Their contribution to the output voltage, together with that of the offset voltage for the second stage is then

$$V_o|_0 = (V_{o1} - V_{o2})k(G + 1) + (k + 1)V_{o3} \tag{3.74}$$

There are several IC instrumentation amplifiers based on the circuit in Figure 3.40. For example, models INA 101, INA 102, INA 104, and INA 110 of Burr-Brown Corp. and model AD 522 of Analog Devices Inc. With these it is easy to achieve a CMRR of 90 dB, at 60 Hz and with a differential gain of 1.

The three-op-amp structure for instrumentation amplifiers is the most popular one. Some IC manufacturers even produce units containing a resistor network, sometimes digitally programmable, playing the role of $R_2$. Then it is possible to change the gain by means of a digital control from the Data Acquisition System. In that case they are called *programmable gain instrumentation amplifiers*.

### 3.5.4 Monolithic Instrumentation Amplifiers

Monolithic integration techniques allow a reduction of production costs for hybrid and modular circuits. For instrumentation amplifiers there are circuit alternatives to those in Figures 3.39 and 3.40 that reduce the redundancy present in them. This does not imply that these circuits are not available in monolithic form. The already mentioned INA 101 is in fact monolithic.

Figure 3.41 shows a simplified version of the internal circuit of model AD 520 from Analog Devices Inc. which was the first monolithic instrumentation

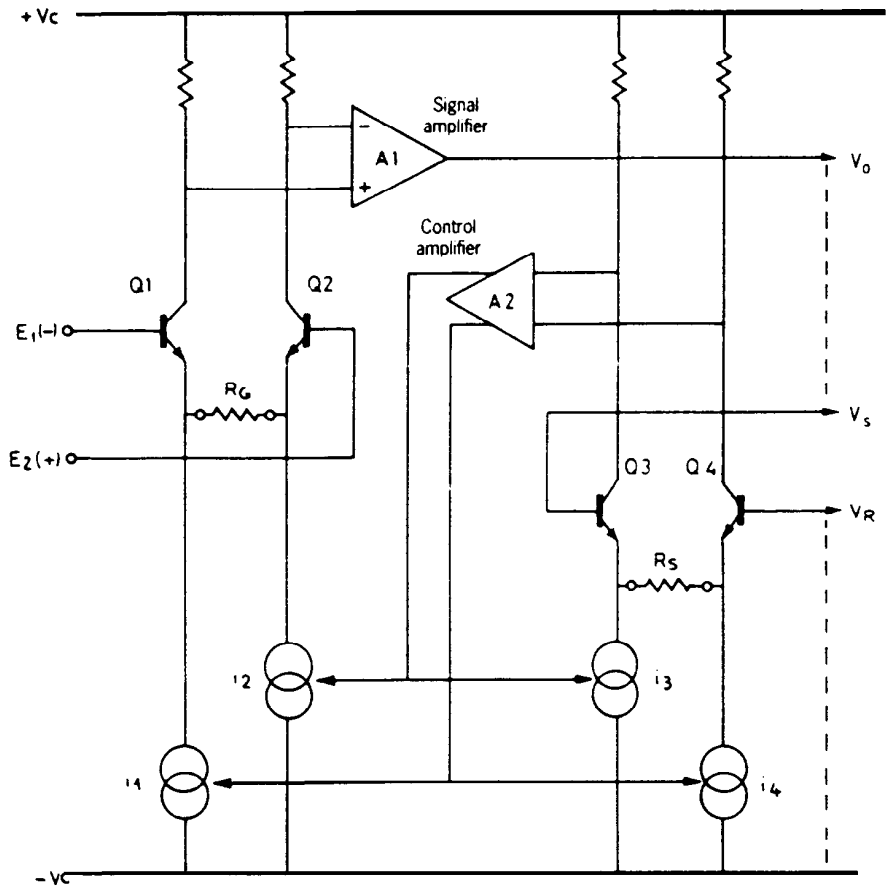


**FIGURE 3.41** Simplified internal structure for a monolithic instrumentation amplifier (Courtesy of Analog Devices Inc.).

amplifier [10]. Actually it has been replaced by improved models, but its circuit allows us to recognize in a simple way the differences between monolithic units and the previous circuits.

When a differential voltage $E_2 - E_1$ is applied to the input, collector currents in $Q_1$ and $Q_2$ are unbalanced by $(E_2 - E_1)/R_G$. Amplifier $A_1$ detects that difference and gives an error voltage between the sense ($S$) and reference ($R$) terminals. This error voltage unbalances collector currents in $Q_3$ and $Q_4$ by $(V_S - V_R)/R_S$. Amplifier $A_2$ detects this difference and adjusts current sources $I_3$ and $I_4$ in order to match collector currents in $Q_3$ and $Q_4$. At the same time $A_2$ adjusts current sources $I_1$ and $I_2$ so that $I_1 - I_2 = I_4 - I_3$. When this situation is achieved, the output voltage is $(E_2 - E_1)R_S/R_G$.

Thus, contrary to instrumentation amplifiers based on two or three op amps, in these monolithic amplifiers the CMRR does not depend on resistor matching but on the matching of current sources.

In addition to those already mentioned, models AMP-01 from Precision Monolithics Inc., AD 524 and AD 624 from Analog Devices Inc., and LM 363 from National Semiconductor Corp. are also monolithic. The time and thermal drifts of their offset voltages and currents, and their noise are even better than those of older hybrid units or modules.

## 3.6 INTERFERENCE

### 3.6.1 Interference Types and Reduction

Interference has been previously defined in Section 1.3.1 as those signals that affect the measurement system as a consequence of the measurement principle used. Here we are concerned with electronic signal conditioning, and therefore we will consider as interference any electric signal present at the output of the system or circuit being considered and coming from a source external to it. Interference problems are not exclusive for electronic measurement systems but are also present in other electronic systems having distinct functions. The interested reader should consider reference [11] for an excellent analysis of interference problems in general, and reference [12] for interference problems in measurement circuits.

Interference is reduced by applying different techniques that depend on the coupling method for the undesired signals. Depending on whether the coupling method is by means of a common impedance, an electric field or a magnetic field, we will respectively speak of resistive, capacitive, and inductive interference.

Figure 3.42 shows a simple circuit illustrating resistive interference. A signal is measured that is ground referenced at a point far from the reference ground for the amplifier, as indicated by the different symbols used. These reference points may be grounded at the respective locations. Therefore, since the ground is used as a return path for leakage currents from electronic equipment, it happens that there is always a voltage difference between different grounds. In industrial environments, at least 1 to 2 V is to be expected.

The use of a differential amplifier connected as shown in Figure 3.43 solves the problem if the total common mode rejection reduces the interference to an output level below the one desired. We assume that the common mode voltage at the op amp inputs due to $V_I$ does not exceed the maximal allowed value. In [13] the use of instrumentation amplifiers for this purpose is described.

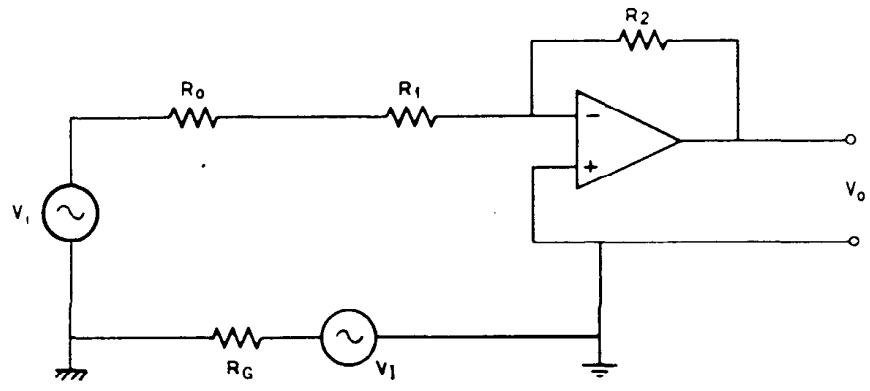


**FIGURE 3.42** Resistive interference due to the drop in voltage produced by stray currents between two distant reference (ground) points.

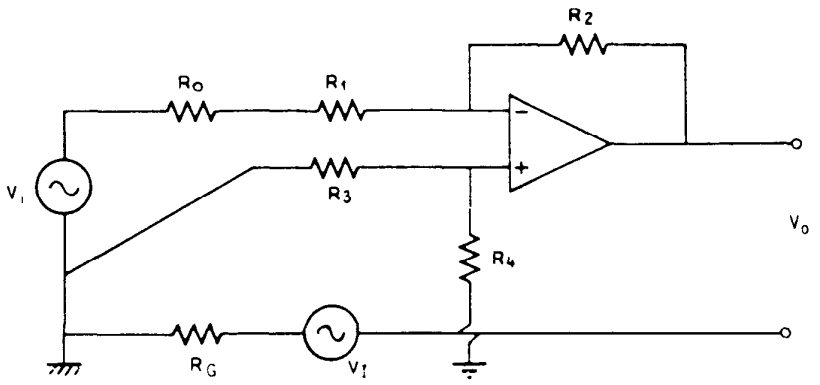


**FIGURE 3.43** Reduction of resistive interference by applying a differential amplifier.

It may happen, however, that either the available CMRR is not high enough or the common mode voltage is too high or just that in addition to the input amplifier there are other circuits connected to the same reference. All these situations call for other solutions that will be described in the following sections.

Figure 3.44 shows the general problem of capacitively coupled interference [11]. Between any pair of conductors there is a finite capacitance. Whenever one conductor is at a certain voltage with respect to a third conductor (the ground plane in Figure 3.44) the second conductor will also increase its voltage with respect to the third conductor.

With the terminology of Figure 3.44, across the equivalent input resistor $R$ presented by the circuit encountering the interference there is a drop in

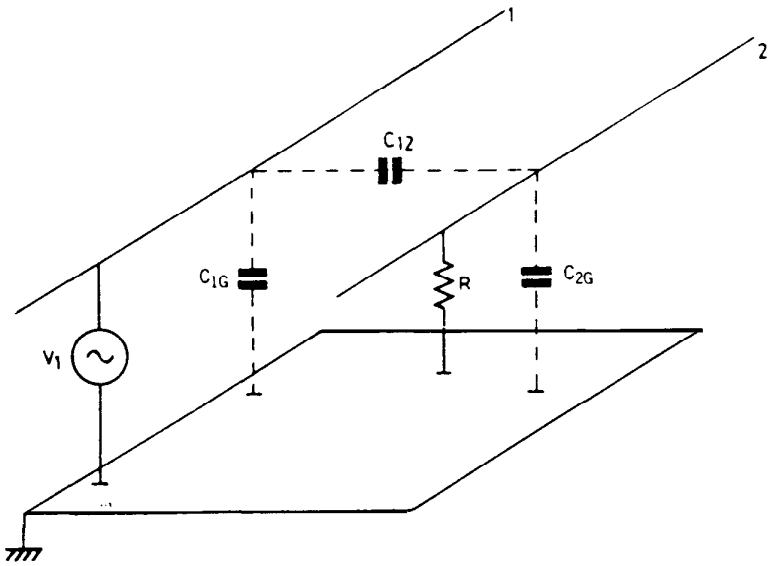


**FIGURE 3.44** Model to describe the problem of capacitive coupling between circuit 1 and circuit 2. (From H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, © 1988. Reprinted by permission of John Wiley, New York.)

voltage due to $V_1$, amounting to

$$V_R = \frac{j\omega RC_{12}}{1 + j\omega R(C_{12} + C_{2G})} V_1 \tag{3.75}$$

If the circuit has a low input resistance, in particular if $R \ll 1/[\omega(C_{12} + C_{2G})]$, then

$$V_R \approx j\omega RC_{12}V_1 \tag{3.76}$$

On the other hand, if $R \gg 1/[\omega(C_{12} + C_{2G})]$, then

$$V_R \approx \frac{C_{12}}{C_{12} + C_{2G}} V_1 \tag{3.77}$$

That is, if $R$ is low, then the interference increases at increasing frequencies, whereas for large $R$ the interference is frequency independent and larger than when $R$ is low. In both cases there is an increased interference for high $C_{12}$ values. In measurement systems the usual interference sources are the 60 (or 50) Hz power lines, and therefore the situation is better described by (3.76), particularly when it is intended to measure the signal from a low output impedance source.

When the reduction of $C_{12}$ that follows from separating both conductors is not enough, then a further reduction of capacitive interference is obtained by shielding conductor 2. It consists of wholly enclosing it by an electrically conductive material connected to a constant voltage. Figure 3.45*a* shows the situation when the shield is connected to ground and when conductor 2 is not in fact totally enclosed, which is the real situation when there is at least one input and one output.

If $R$ has a much larger impedance than $C_{2G}$ at the frequencies considered, the equivalent circuit is that in Figure 3.45*b*. In that case, if the impedance of the shield to ground connection is low enough and $Z_S \ll 1/\omega C_{1S}$, then we have

$$V_R \approx \frac{C_{12}}{C_{12} + C_{2S} + C_{2G}} V_1 \tag{3.78}$$

where $C_{12}$ is now much smaller than when no shield is used because it concerns only those segments outside of the shield (which is considered as perfect). Then the final interference will be greatly reduced. In practice, conductors are enclosed in a wire mesh whose effective shielding or coverage factor depends on how closely it is woven. In view of the simplifications leading to (3.78) and by considering Figure 3.45*b*, we can conclude that shielding efficiency depends on the relative value for $Z_S$ as compared to $C_{1S}$.

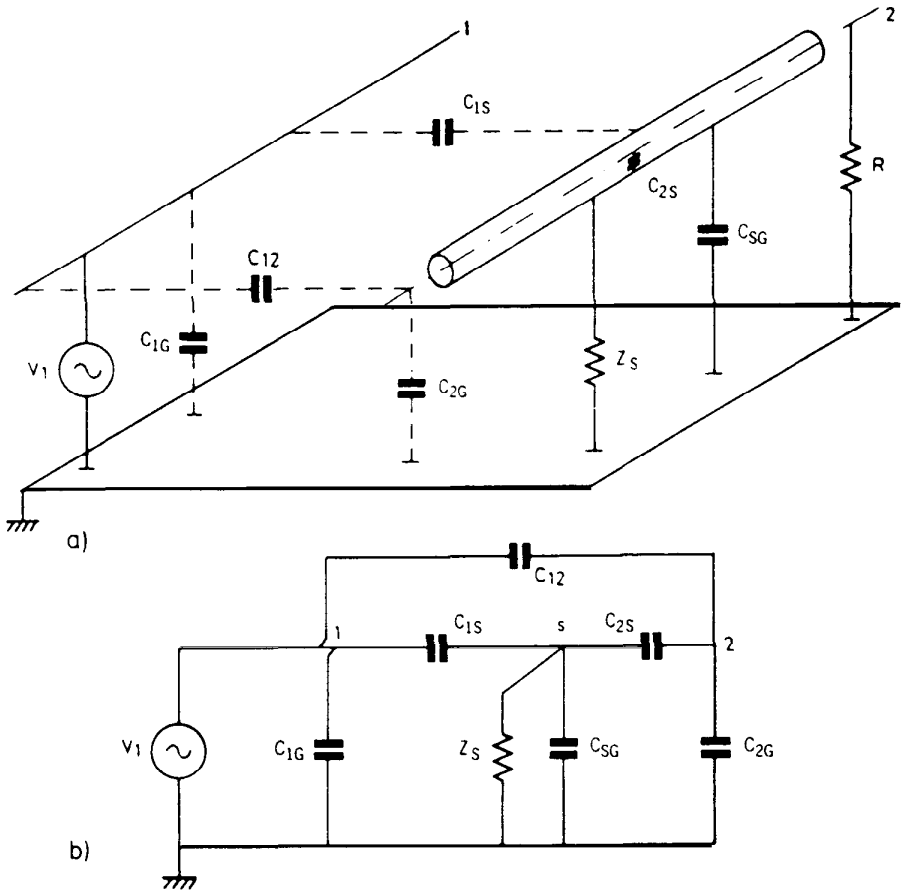


**FIGURE 3.45** (*a*) Electric shielding of conductor 2 by a shield connected to a constant voltage (ground in this case) and (*b*) equivalent circuit for its analysis when $R$ is large. (From H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, © 1988. Reprinted by permission of John Wiley, New York.)

In case $R$ is not large enough but $Z_S$ is small enough, we obtain

$$V_R \approx \frac{j\omega RC_{12}}{1 + j\omega R(C_{12} + C_{2S} + C_{2G})} V_1 \tag{3.79}$$

For $R \ll 1/[\omega(C_{12} + C_{2S} + C_{2G})]$, then

$$V_R \approx j\omega RC_{12}V_1 \tag{3.80}$$

That is, the interference also depends on $C_{12}$ which is very small.

It is very important to recognize that in order for a shield to be effective, it must be connected to a constant voltage. Otherwise, even though $C_{12}$ were zero, an interference may result. For the case analyzed, if we take $Z_S = \infty$, and we suppose, for example, that for the situation where $R$ is large, we have

$$V_R \approx V_S \approx V_1 \frac{C_{1S}}{C_{1S} + C_{SG}} \tag{3.81}$$

That is, if $C_{1S}$ is large, the resulting interference may be even larger than the case when there is no shielding. The shield must thus be connected to a constant voltage. We must decide which end of the shield to connect to which voltage. We will answer these questions in the following sections.

We say that there is an inductive coupling or a magnetic interference when the magnetic field produced by the current in a circuit induces a voltage in the signal circuit being considered. The relationship between the current in a circuit and the magnetic flux it produces in another is expressed by means of the mutual inductance $M$,

$$M = M_{12} = M_{21} = \frac{\Phi_{12}}{I_1} = \frac{\Phi_{21}}{I_2} \tag{3.82}$$

In case of a variable magnetic flux, **B**, the voltage $V_2$ induced in a loop with area **S** is given by

$$V_2 = -\frac{d}{dt}\int_S \mathbf{B} \cdot d\mathbf{S} \tag{3.83}$$

where **B** and **S** are vector quantities. If the loop is static and $B$ changes sinusoidally at frequency $\omega$, we have,

$$V_2 = j\omega BS \cos\theta \tag{3.84}$$

where $\theta$ is the angle between **B** and **S**.

Therefore, in a way similar to the case of capacitive interference, a current $I_1$ circulating along a conductor induces an interfering voltage $V_2$ in a circuit such as the one in Figure 3.46, as given by (3.84). But in the present case it happens that the interference is always proportional to the frequency (for capacitive coupled interferences there was proportionality only at low frequencies) and is independent of the impedance presented by the receiving circuit (capacitive interference increased with increasing circuit impedance).

If a reduction in $B$ is not possible, the usual solution in order to reduce magnetic interferences is by reducing the area $S$. This is done by twisting leads or by placing the conductor close to the return path, if the return path is not a wire conductor. In some instances it is also possible to reduce the cos $\theta$ term by reorienting the circuit. Note that a conductive shield around 2 does not solve the problem: The shield will be raised to a voltage level $V_S = j\omega M_{1S} I_1$, or we will have $V_S = 0$ if one end is tied to ground, and that is all.

### 3.6.2 Signal Circuit Grounding

A ground is a point or equipotential plane that serves as a reference for the voltages in a circuit or system. When grounding a circuit or system, we must minimize the noise voltages generated by currents flowing between circuits

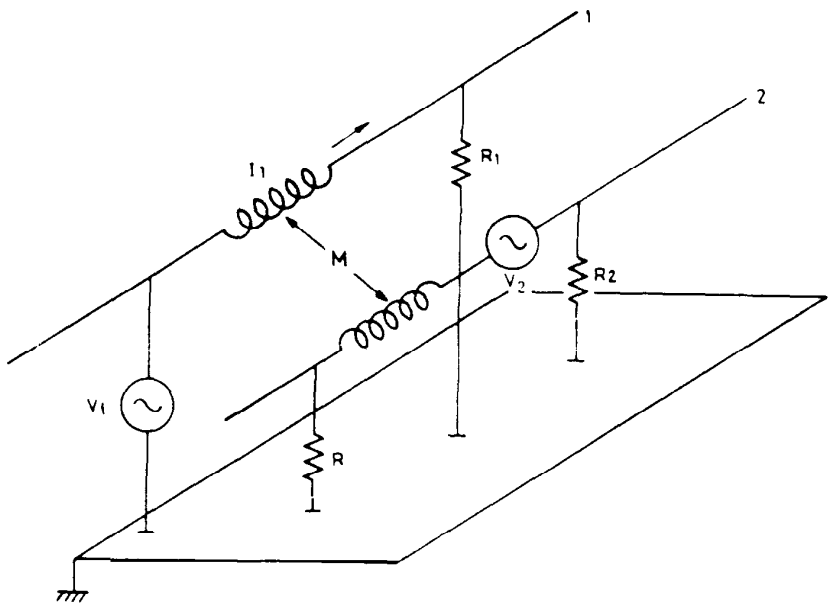


**FIGURE 3.46** Model to describe the problem of inductive coupling between circuit 1 and circuit 2. (From H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, © 1988. Reprinted by permission of John Wiley, New York.)

through a common impedance. We must avoid ground loops because they are susceptible to magnetic interference and to voltage differences between different grounding points. Figure 3.47 shows three different grounding methods and the respective circuits to analyze them.

With the series ground connection method, supply currents for each circuit produce drops in voltage that result in a different voltage reference for each circuit, namely,

$$V_A = (I_1 + I_2 + I_3)Z_1 \tag{3.85}$$

$$V_B = (I_1 + I_2 + I_3)Z_1 + (I_2 + I_3)Z_2 \tag{3.86}$$

$$V_C = (I_1 + I_2 + I_3)Z_1 + (I_2 + I_3)Z_2 + I_3Z_3 \tag{3.87}$$

Because the output signals for each circuit are voltage-referenced to different points, this interference source may be important. Therefore this grounding method should not be used whenever there are circuits with dissimilar supply currents. In any case the more susceptible stages should be placed close to the common reference point.

The method of parallel grounding at a single point, shown in Figure 3.47*b*, requires a more involved physical layout but overcomes the problem pointed out for series grounding. Therefore it is the preferred method for low-frequency grounding.

For high-frequency circuits (>10 MHz) multiple grounding points as shown in Figure 3.47*c* are preferred to single-point grounding because a lower ground impedance is obtained. The impedance of the ground plane can be further reduced by plating its surface.

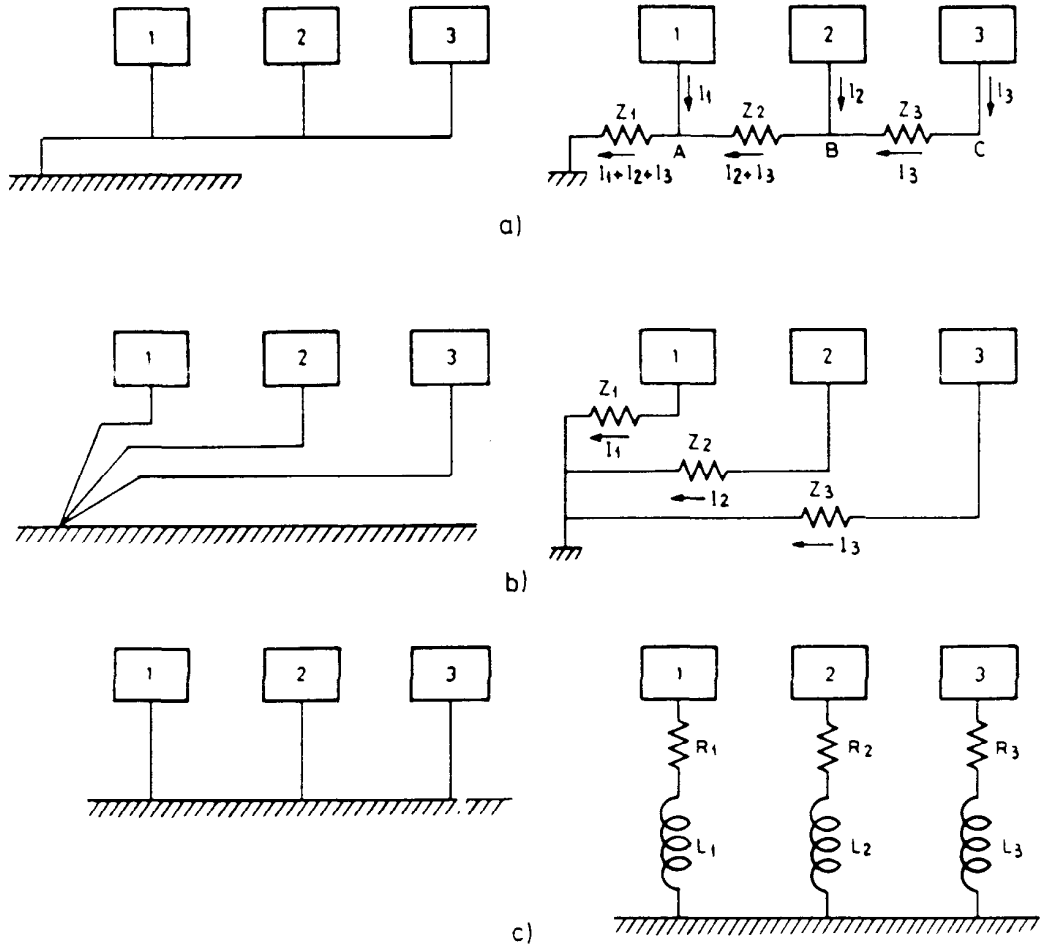


**FIGURE 3.47** Different grounding methods and equivalent circuits to analyze them: (*a*) single-point series grounding method; (b) single-point parallel grounding method; (*c*) Multipoint parallel grounding method. (From H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, © 1988. Reprinted by permission of John Wiley, New York.)

### 3.6.3 Shield Grounding

Section 3.6.1 points out that the shield of a conductor is effective only when it is connected to a constant voltage. When shielding amplifiers, the shield must be connected to the reference voltage for the enclosed circuit, whether it is grounded or not. Figure 3.48*a* shows the correct connection.

If the shield were not connected or connected to a different voltage, there would be a parasitic feedback from the amplifier output to its input that could even lead to oscillations. Figure 3.48*b* shows the case where the shield is left unconnected. Figure 3.48*c* shows the equivalent circuit for its analysis.

Figure 3.48*d* shows that connecting the reference point for an amplifier to ground when its shield is not connected does not solve the problem of external interference. Figure 3.48*e*, the equivalent circuit for that case, shows that in order to have minimal coupling from $V_i$ to the shield, $X_{C_{2S}}$ must be very small; that is, it must be short-circuited.

When grounding amplifier shields, the internal circuit must be connected to the shield at a single point, for example, as shown in Figure 3.49*a* for the

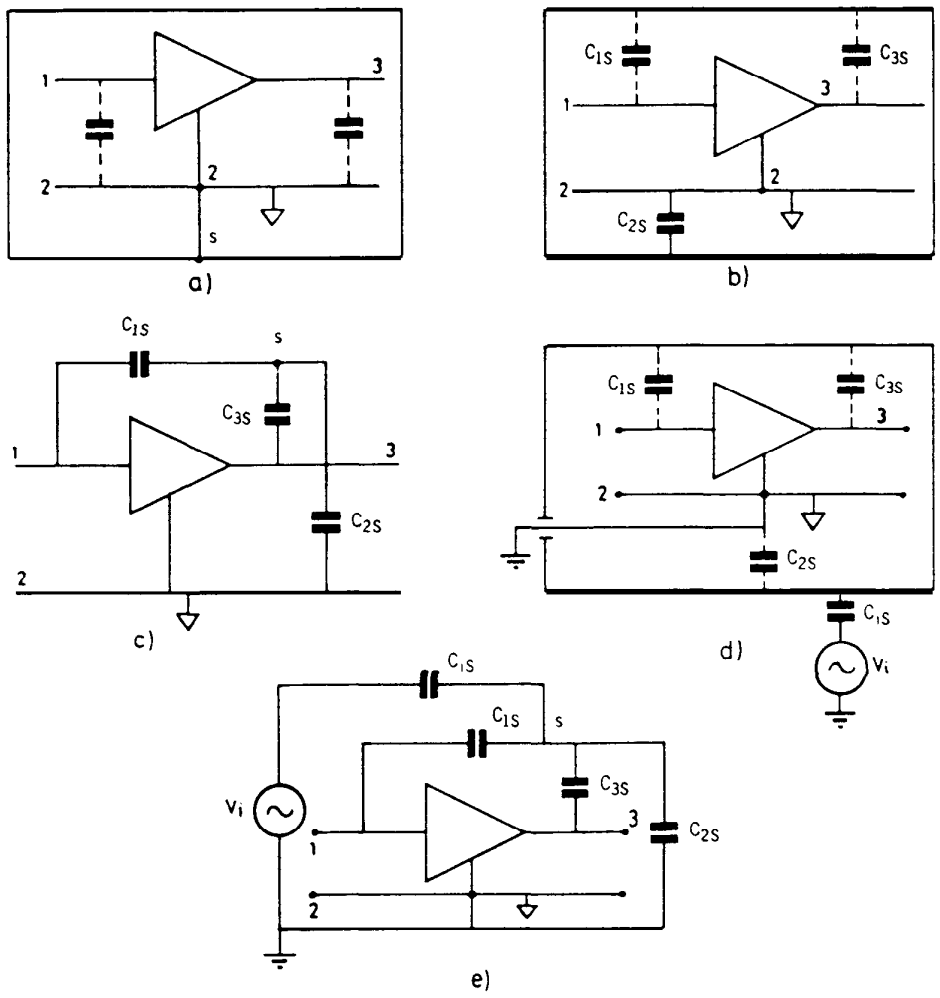


**FIGURE 3.48** Amplifier shielding: (*a*) correct shield connection; (*b*) incorrect situation (shield unconnected); (*c*) circuit to analyze the previous case; (*d*) grounding does not solve the problem; (*e*) circuit to analyze the previous case.

case of a grounded shield intended to reduce power line interference. Otherwise, if there is more than one point connecting the circuit to the shield, resistive interference such as shown in Figure 3.49*b* may appear across $V_{AB}$.

We must choose the single connection point carefully in order to avoid currents coupled to the shield from circulating along the same path as signal currents. For example, if the signal were grounded and the shield-amplifier connection were as shown in Figure 3.50*a*, then the interfering voltage $V_i$ would couple through $C_{iS}$ a current to ground via $S$–2–$b$, that is, it would share the segment 2–$b$ with the signal.

Thus we should choose a grounding scheme such as the one in Figure 3.50*b* where the reference point for the amplifier ("2") is connected to the shield not directly in the amplifier but at the signal source. Then external interference does not share any path with the signal. The situation in Figure 3.50*b* can be described by saying that the amplifier has a "floating" input, that is, point 2 is not grounded within the amplifier.

When grounding a cable shield with a single ground connection, we must

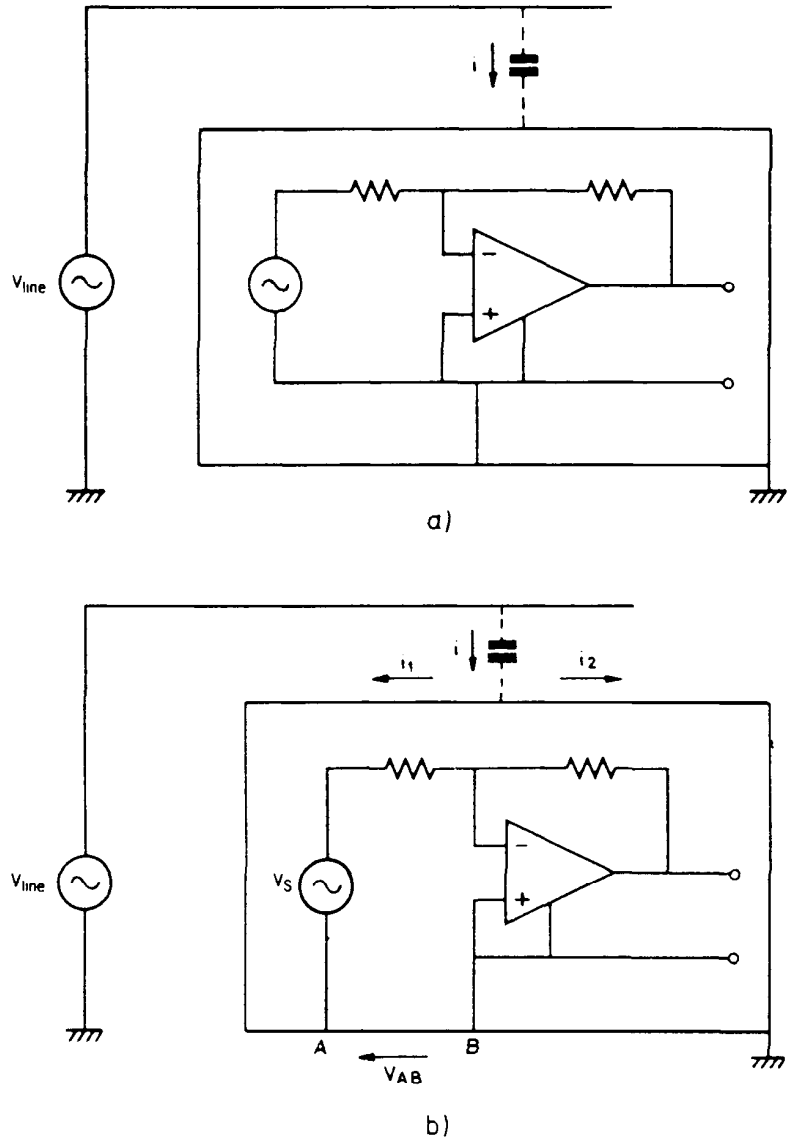


**FIGURE 3.49** Shield and circuit must be connected at a single point (*a*); otherwise, resistive interference $V_{AB}$ may appear (*b*).

decide which end to connect: the one at the signal end or the one at the amplifier end.

If the signal is not grounded and the amplifier is, then the best solution is to connect the shield to the input reference terminal for the amplifier, as indicated in Figure 3.51. If the shield were connected to the reference terminal at the signal side (connection *A*, dashed), all interference currents coupled to the shield would flow to ground along one of the signal lead wires (the one at terminal 2; the amplifier is assumed to have a high input impedance). If connection *B* were used, the interfering voltage at the input of the amplifier would be

$$V_{12} = (V_{G1} + V_{G2}) \frac{C_{1S}}{C_{1S} + C_{12}} \tag{3.88}$$

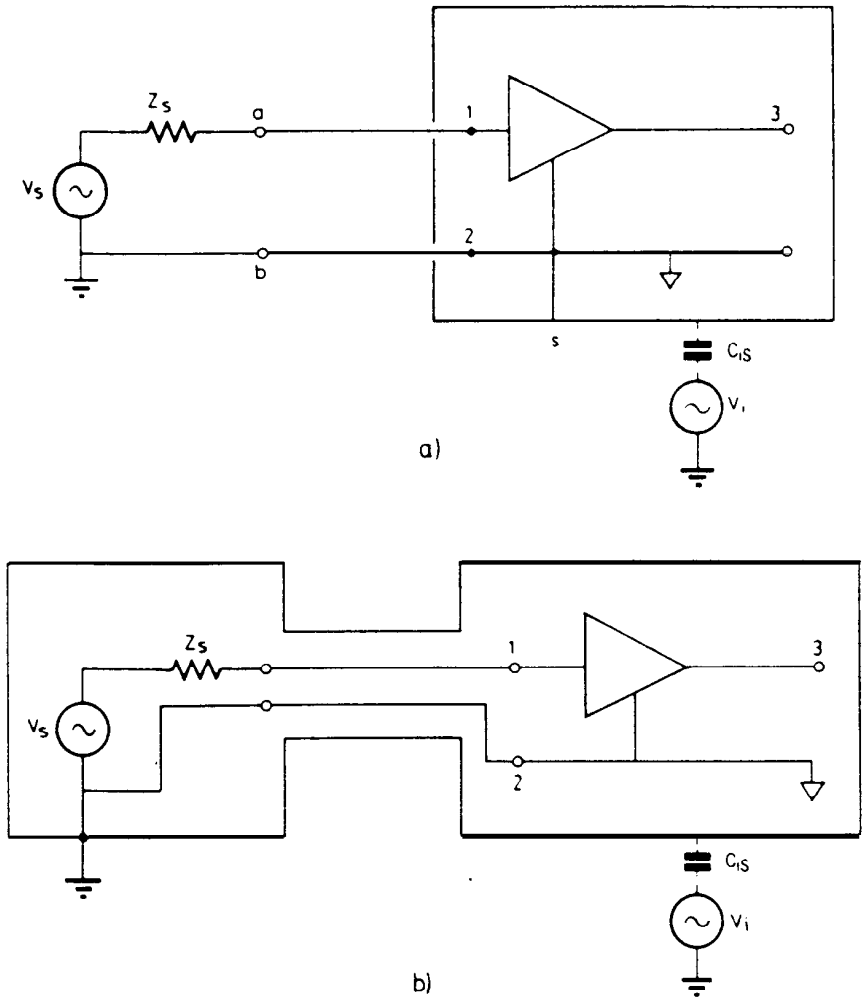


**FIGURE 3.50** Selection of the grounding point for a shield. In case (*a*) the interference induces a current that shares a path 2–*b* common to the signal; in case (*b*) external interference follows a path different than that of the signal.

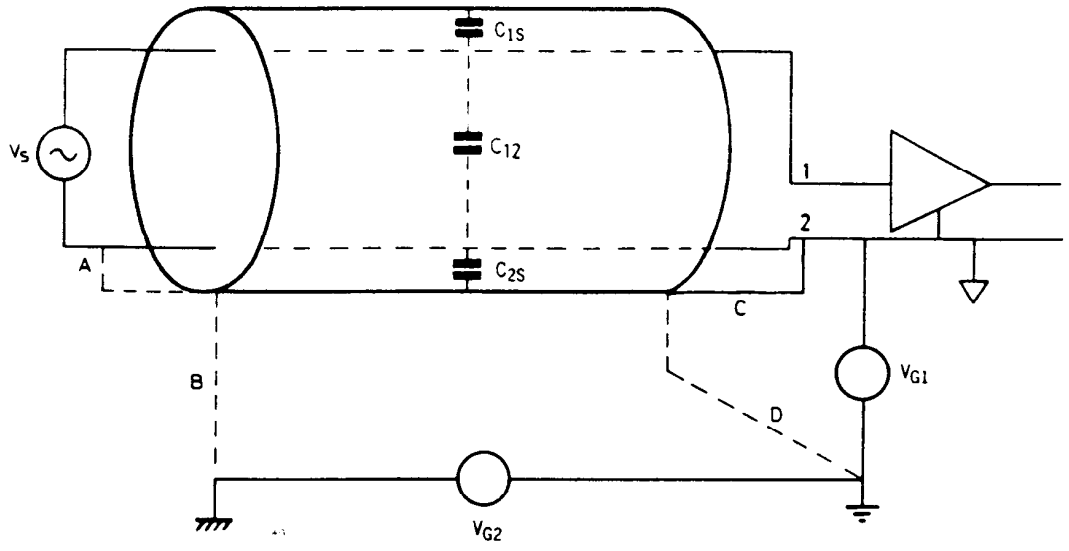


**FIGURE 3.51** Ground connection for a shield cable when the signal is not grounded and the amplifier is. The appropriate connection is indicated by a solid line. (From H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, © 1988. Reprinted by permission of John Wiley, New York.)

If the shield were grounded at the amplifier side, connection $D$, the interfering voltage would then be

$$V_{12} = V_{G1} \frac{C_{1S}}{C_{1S} + C_{12}} \tag{3.89}$$

Therefore, if the signal source is not grounded but the amplifier is, then the shield must be connected to the reference terminal for the amplifier, even if it is not grounded.

If the signal is grounded but the amplifier input is not, then the situation is different and so is the solution. Now it is better to ground the shield on the signal source end, as shown in Figure 3.52. If instead of that it were connected to ground at the signal end (connection $B$), we would have

$$V_{12} = V_{G1} \frac{C_{1S}}{C_{1S} + C_{12}} \tag{3.90}$$

We should not connect the shield to the reference terminal at the amplifier input because then all shield coupled currents would flow to ground along one of the signal lead wires. If connection $D$ is used, the input interfering voltage would be

$$V_{12} = (V_{G1} + V_{G2}) \frac{C_{1S}}{C_{1S} + C_{12}} \tag{3.91}$$

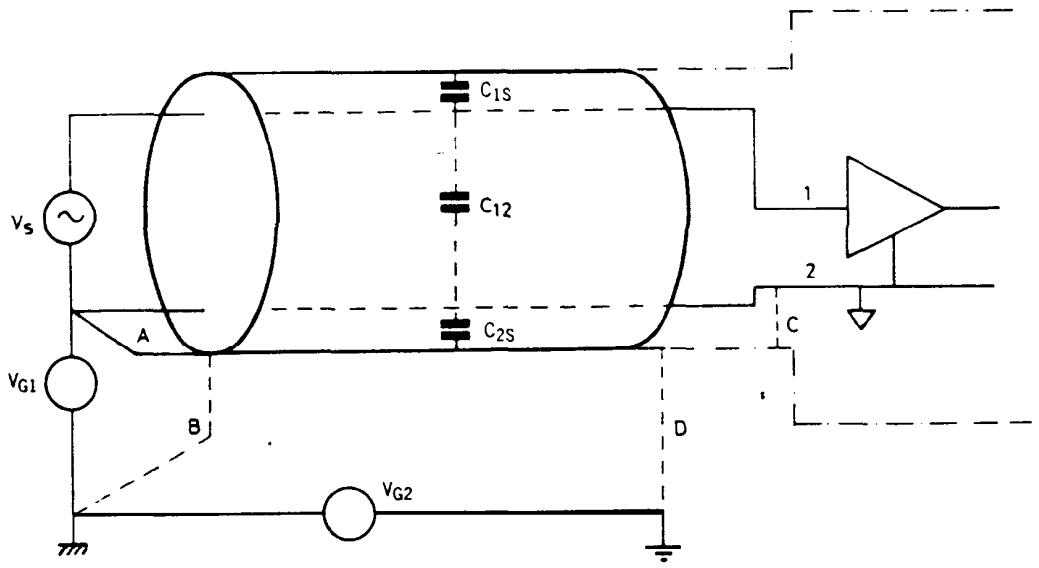


**FIGURE 3.52** Ground connection for a shield cable when the signal is grounded but the amplifier is not. The appropriate connection is indicated by a solid line. (From H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, © 1988. Reprinted by permission of John Wiley, New York.)

Note that the situation in Figure 3.52 connection *A* is the same as the one in Figure 3.50, but now we have included the possibility of a nonperfect grounding connection and the presence of an interfering voltage between the signal reference point and ground, which are connected by a low-value impedance.

If both the signal source and the amplifier are grounded, perhaps the compromise solution is to connect the shield to ground at both ends. But depending on the difference in voltage between grounding points and on the magnetic coupling to the newly created ground loop, the resulting interference may be increased. If this is the case, the loop must be opened by using differential input amplifiers or isolation amplifiers.

### 3.6.4 Isolation Amplifiers

An isolation amplifier is an amplifier that offers an ohmic isolation between its input and output terminals. This isolation must have low leakage and a high dielectric breakdown voltage, that is, high resistance and low capacitance. Typical values for these are, respectively, 10 TΩ and 10 pF.

The interest in isolation amplifiers arises first from the fact that all instrumentation amplifiers show a limited capability for withstanding high common mode voltages, the usual limit being about 10 V. For example, a CMRR of 100 dB seems to imply that a 100 V common mode voltage would give a mere 1 mV at the output, but in fact a component will break down if such a voltage is applied to its input.

Measurement situations encountering high common mode voltages arise in obvious cases such as in a high voltage device. They may also arise in unsuspected cases as a sensor bridge supplied by more than 20 V or when two grounding points are involved whose voltage difference amounts to several tens of volts.

In isolation amplifiers there is no ohmic continuity from the input reference terminal (input common, input ground) to the output reference terminal (output common, output ground). The input common is also independent of the reference terminal of the power supply (supply common, supply ground). In some cases the power supply is also independent from the output common. Figure 3.53 gives some of the symbols used for isolation amplifiers.

Signals and supply power are coupled by a transformer from one part to the other of isolation amplifiers. Signals can also be coupled by optical or capacitive means (optocouplers, capacitors). A modulated carrier is used through the isolation barrier in order to improve linearity. The ability for rejecting those voltages appearing between the input common and the other common terminals is quantified by means of the isolation mode rejection ratio (IMRR), which is defined in a way similar to the CMRR.

Note that an isolation amplifier is not an op amp, a differential amplifier, or an instrumentation amplifier. In fact there are models whose input stage is

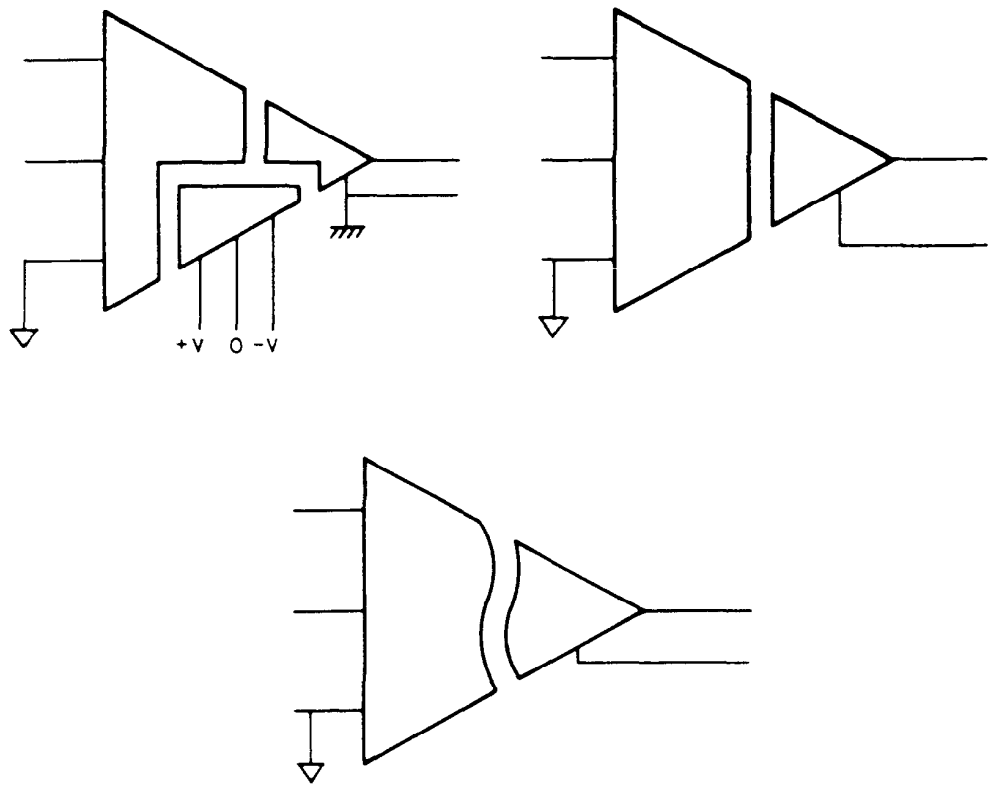


**FIGURE 3.53** Different symbols used for isolation amplifiers.

an uncommitted op amp that can be connected as needed; other models have an input stage that is a two-op-amp instrumentation amplifier; still others implement the three-op-amp circuit and need a single external resistor for gain setting.

Figure 3.54 shows the application of an isolation amplifier to interface a grounded recording instrument with a sensor bridge whose power supply is also grounded but at a remote point and with a ground voltage different from that of the recorder. In this application the input stage must be differential in order to reject the common mode voltage arising at the bridge output be-

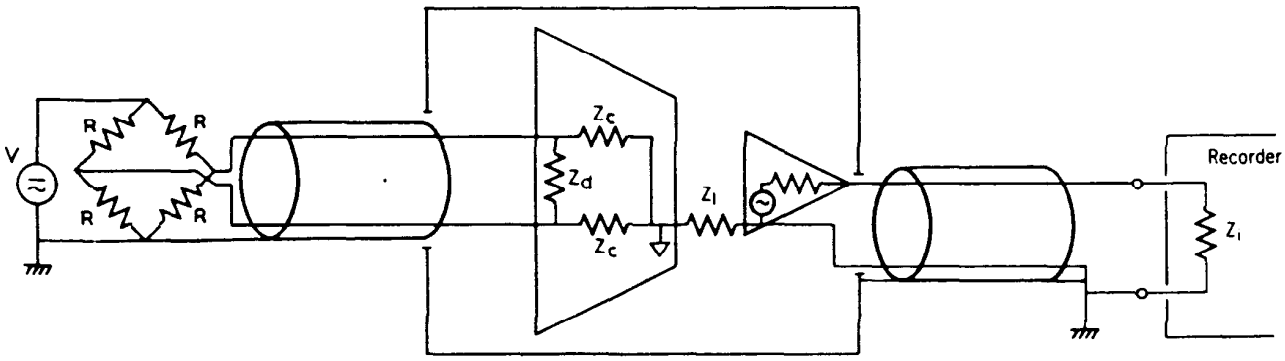


**FIGURE 3.54** Application of an isolation amplifier to interfacing a sensor bridge with grounded supply and a recorder also grounded. We do not show the connections necessary for biasing the amplifier.

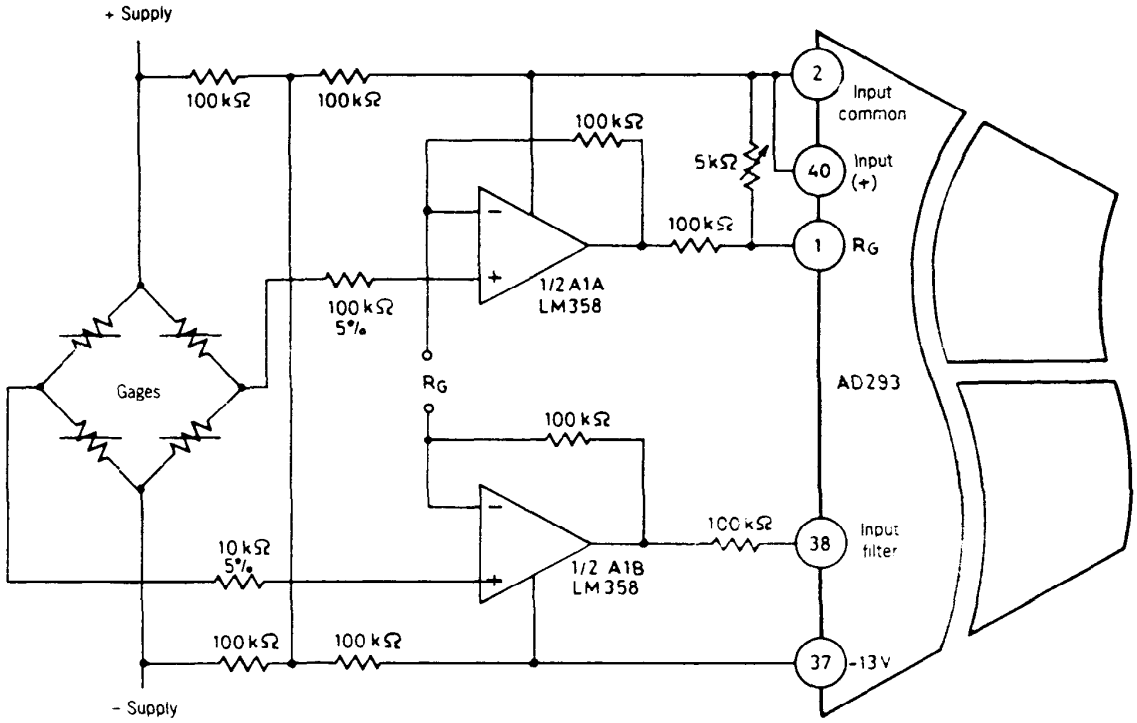


**FIGURE 3.55** Amplifier for a sensor bridge based on the isolation provided by an isolation amplifier that powers an input differential stage (Courtesy of Analog Devices Inc.).

cause of the supply voltage. The voltage at the amplifier output induced by the difference in voltage between the grounding points is obtained by dividing this voltage difference by the IMRR.

Isolation amplifiers are available in integrated circuit form. They are not usually precision devices. Nevertheless, they can be applied to precision sensor signal conditioning, provided they include an isolated supply at the input side able to supply a high-quality preamplifier, for example, a low drift amplifier or a differential stage like the one shown in Figure 3.55.

## 3.7 PROBLEMS

1. The output signal of a potentiometer is connected to a recorder whose input resistance is 10 kΩ. The nonlinearity error due to loading effect must be lower than 1% of full-scale output. A series of 5-W potentiometers with resistance from 100 to 10,000 Ω in 100 Ω increments is available. What unit would give the maximal sensitivity without exceeding any of the imposed restrictions? What would its sensitivity be if they were single-turn models (360°)?

2. A method of reducing the nonlinearity error due to meter loading effect in a potentiometer is by placing a resistor in series with the power supply

and the potentiometer. Determine what resistor value yields the maximal nonlinearity error with this method and give the expression for the error as a function of resistance ratios.

3. A given quantity $x$ ranging from $x = 0$ to $x = 10$ is to be measured by means of a linear resistance sensor such that for $x = 0$ its resistance is 1000 Ω and for $x = 10$ it is 1100 Ω. In order to obtain an electric output signal corresponding to $x$, the sensor is placed in a resistance bridge supplied by a dc voltage whose value is limited by the maximal power dissipated by the sensor specified at 25 mW.
   **a.** Assume that for $x = 0$ the bridge is balanced and that bridge resistors are chosen for the maximal bridge sensitivity for a given supply voltage. Calculate the maximal relative error that would be produced when the bridge output is considered to be linearly dependent on $x$.
   **b.** Assume a balance condition for $x = 0$ and that the relative error must be kept below 1%. What values should the bridge resistors have?
   **c.** Assume that $x$ is a force, that the bridge is supplied by the maximal acceptable voltage, and that its output is linear. What would the sensitivity be for the previous case?
   **d.** Assume the bridge output is linear. What would the sensitivity be if the four bridge resistors were equal? Explain why it is different from the sensitivity in the previous case.

4. Assume that in the previous problem the three fixed resistors are valued 1000 Ω, that the sensitivity is 25 mV/N, and that the output voltage is measured with an instrumentation amplifier where a 0 to 5 V output should correspond to the range $x = 0$ to $x = 10$.
   **a.** Calculate the gain $G$ for an ideal amplifier.
   **b.** Assume an amplifier with a CMRR = 70 dB + 20 log$(G + 1)/2$ and equal input differential and common mode resistances. Assume that other error sources (offset, drifts, noise) are negligible. Then the value for $G$ calculated in the previous part will not give 5 V when $x = 10$, but error voltages will be present. If the bridge supply and the amplifier have a common reference terminal, calculate the relative error when $x = 10$ as a function of the input differential mode resistance. Would this error be zero if that resistance were infinite? Why?

5. Assume that in the example in Section 3.4.1 the bridge output is connected to an instrumentation amplifier. Calculate the minimal value for the input differential and common mode resistances and the CMRR so that their finite values yield an error negligible with respect to the specified errors for the design of the bridge (0.5% of reading plus 0.2% of full-scale value).

6. A given platinum RTD probe has a resistance of 1000 Ω at 25°C, a temperature coefficient $\alpha = 0.4\%/\text{K}$, and a thermal dissipation constant of

5 mW/K. Use it to design a thermometer for the range from 0 to 100°C having maximal possible sensitivity but without exceeding a 1% relative error of the output voltage. Use a bridge arrangement and assume that its output is measured with an ideal voltmeter.

**7.** The circuit in Figure P3.1 is proposed for a thermometer based on the TSP 102 sensor (a linearized PTC) whose resistance at 25°C is 1000 Ω and temperature coefficient 0.7%/°C. Design the values for $R$ and $R_2$ in order to measure temperatures from −10°C to +50°C.

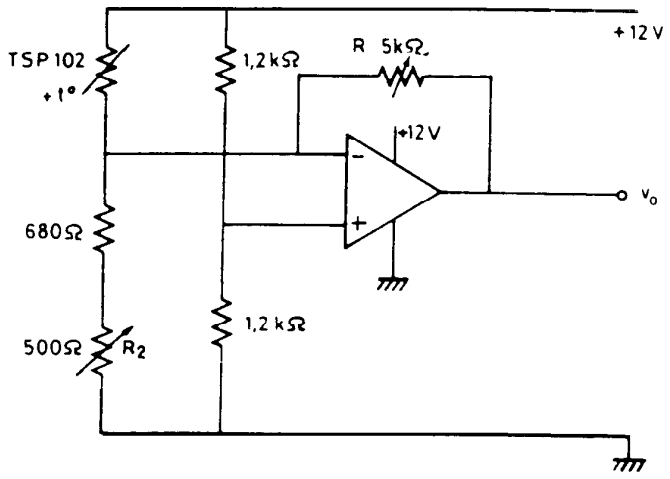


**FIGURE P3.1**

**8.** Use the circuit in Figure P3.2 to measure temperatures in the range from 0°C to 40°C, with a corresponding output voltage from 0 to 12 V. The sensor is a linearized PTC thermistor having $\alpha = 0.75\%/K$, a resistance of 2000 Ω at 25°C, and a maximal acceptable current of 1 mA. Assume that the op amp is ideal.

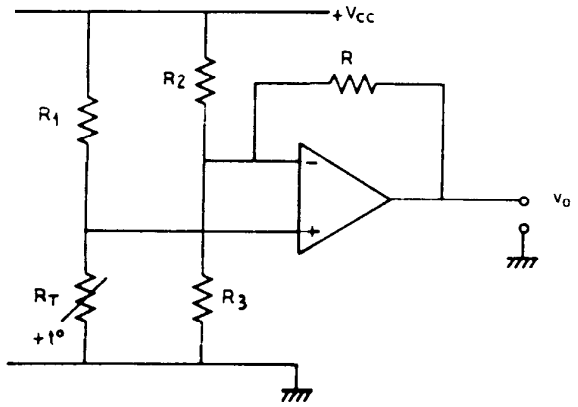


**FIGURE P3.2**

**a.** Design the circuit components in order to obtain the output signal desired.

**b.** Determine the temperature where the nonlinearity error is maximal, and calculate this error.

9. The circuit in Figure P3.3 is a pseudobridge based on two equal linear resistance sensors. Assume that the op amp is ideal, and show that the output voltage is directly proportional to the measured quantity.

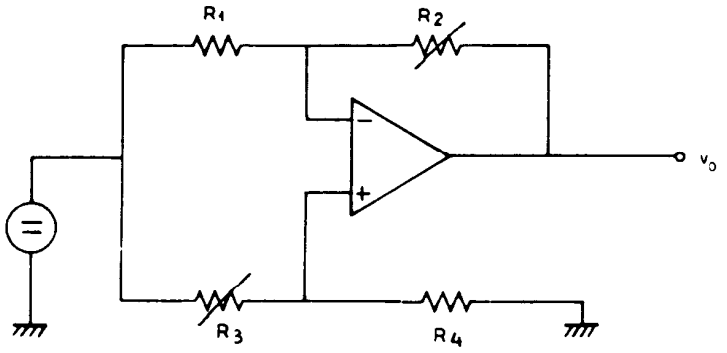


**FIGURE P3.3**

## REFERENCES


1. E. O. Doebelin. *Measurement Systems Application and Design*, 4th ed. New York: McGraw-Hill, 1990.
2. C. D. Todd (Bourns Inc.). *The Potentiometer Handbook*. New York: McGraw-Hill, 1975.
3. J. Schoeff and D. Soderquist. *Differential and Multiplying Digital-to-Analog Converter Applications*. Application Note 19. Santa Clara, CA: Precision Monolithics Incorporated.
4. K. S. Lion. *Elements of Electrical and Electronic Instrumentation*. New York: McGraw-Hill, 1975.
5. Burr-Brown Corp. Tame transducer bridge errors with op-amp feedback control. In *The Handbook of Linear IC Applications*. Tucson, AZ, 1987.
6. D. H. Sheingold. *Transducer Interfacing Handbook*. Norwood, MA: Analog Devices Inc., 1980.
7. R. M. Stitt. Precision voltage references outgrow temperature-stabilizing ovens. *Electronics* **56** (23), (1983), 145–147.
8. J. Szynowski. CMRR analysis of instrumentation amplifiers. *Electronics Letters* **19,** 14 (July 7, 1983), 547–549.
9. Burr-Brown Corp. Monolithic difference amp eases the design of a variety of circuits. In *The Handbook of Linear IC Circuits*. Tucson, AZ, 1987.
10. J. R. Riskin. *A User's Guide to IC Instrumentation Amplifiers*. Norwood, MA: Analog Devices Inc., 1978.
11. H. W. Ott. *Noise Reduction Techniques in Electronic Systems*, 2d ed. New York: Wiley, 1988.
12. R. Morrison. *Instrumentation Fundamentals and Applications*. New York: Wiley, 1984.
13. Burr-Brown Corp. Instrumentation amplifiers shift signals from noise. In *The Handbook of Linear IC Circuits*. Tucson, AZ, 1987.
14. C. D. Cooper. Bridge-to-computer data acquisition system with feedback nulling. *IEEE Trans. Instrum. Meas.* **39,** (1990), 531–534.