Memory Device Evolution

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Micron

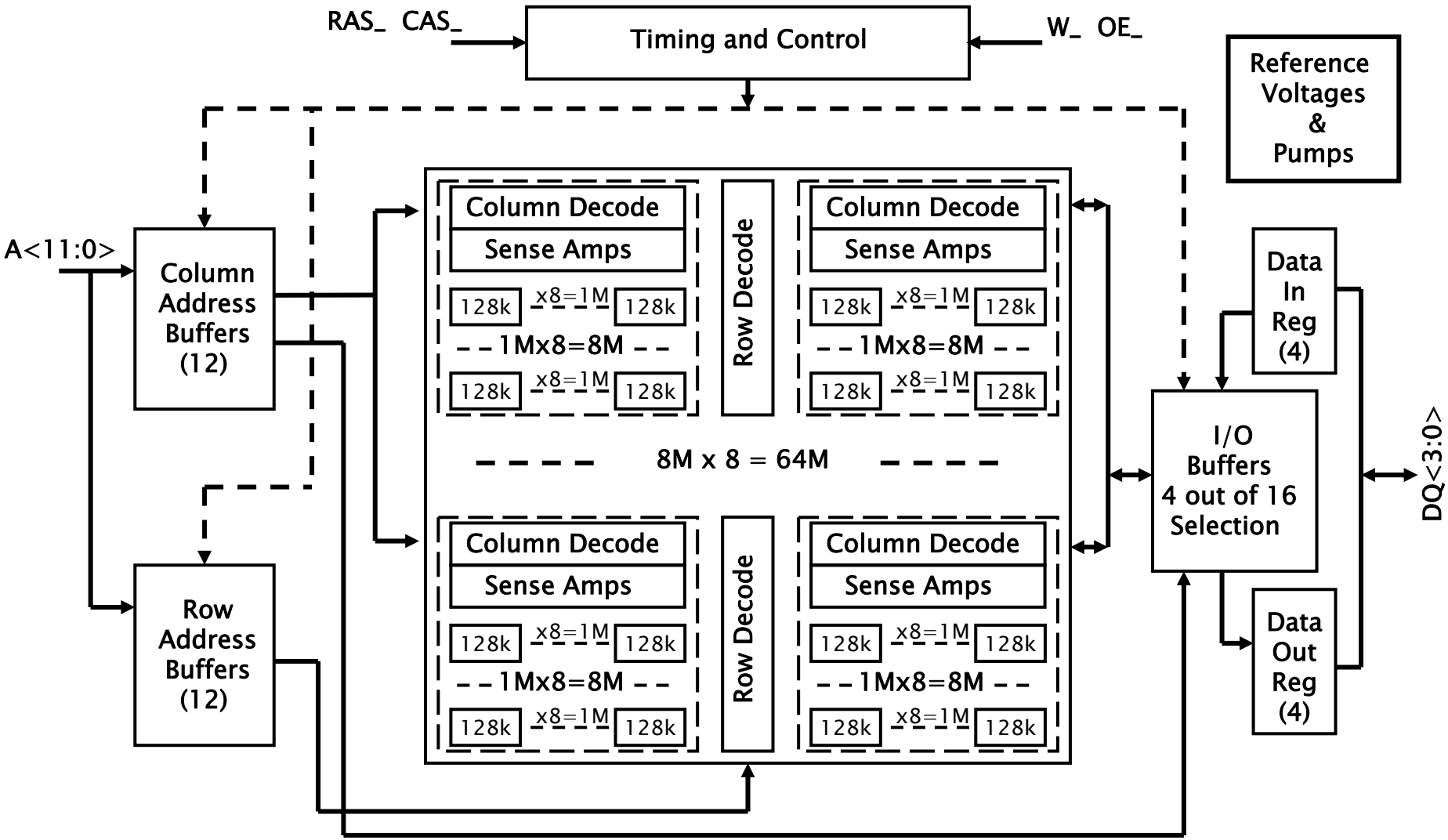
Agenda

- Random access memories
  - A quick comparison of technologies
  - Details of external memory technologies
    - Solutions for low-power and mobile applications
    - Solutions for high performance
- Nonvolatile memories
  - A quick comparison of technologies
  - Details of external memory options

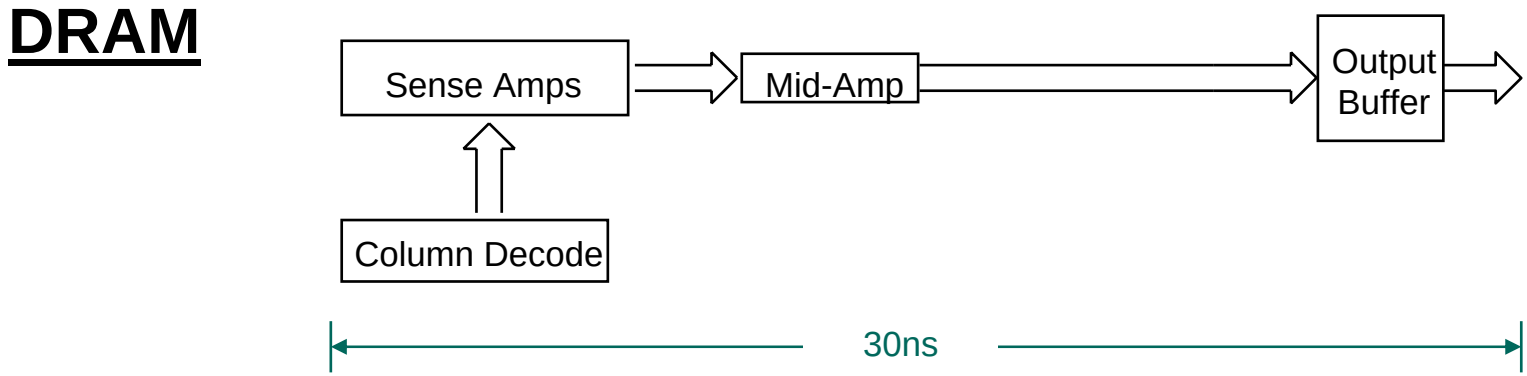
Random Access Memory Technologies
(Relative Comparison)

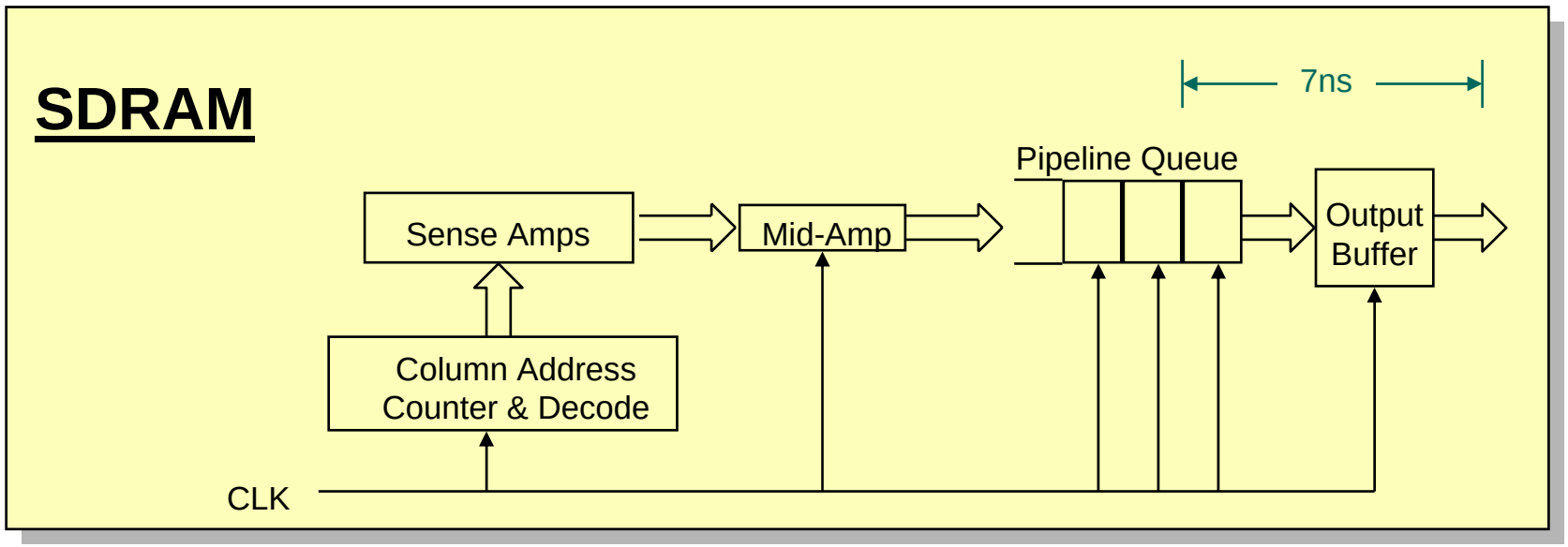
Technology	High-Speed SRAM	Low-Power SRAM	Embedded DRAM	External DRAM	Pseudo-Static RAM
Power					
Density					
Area					
Speed					
Other Features			Wide busses	High density	Medium density
Costs					

Architecture of a DRAM Memory device

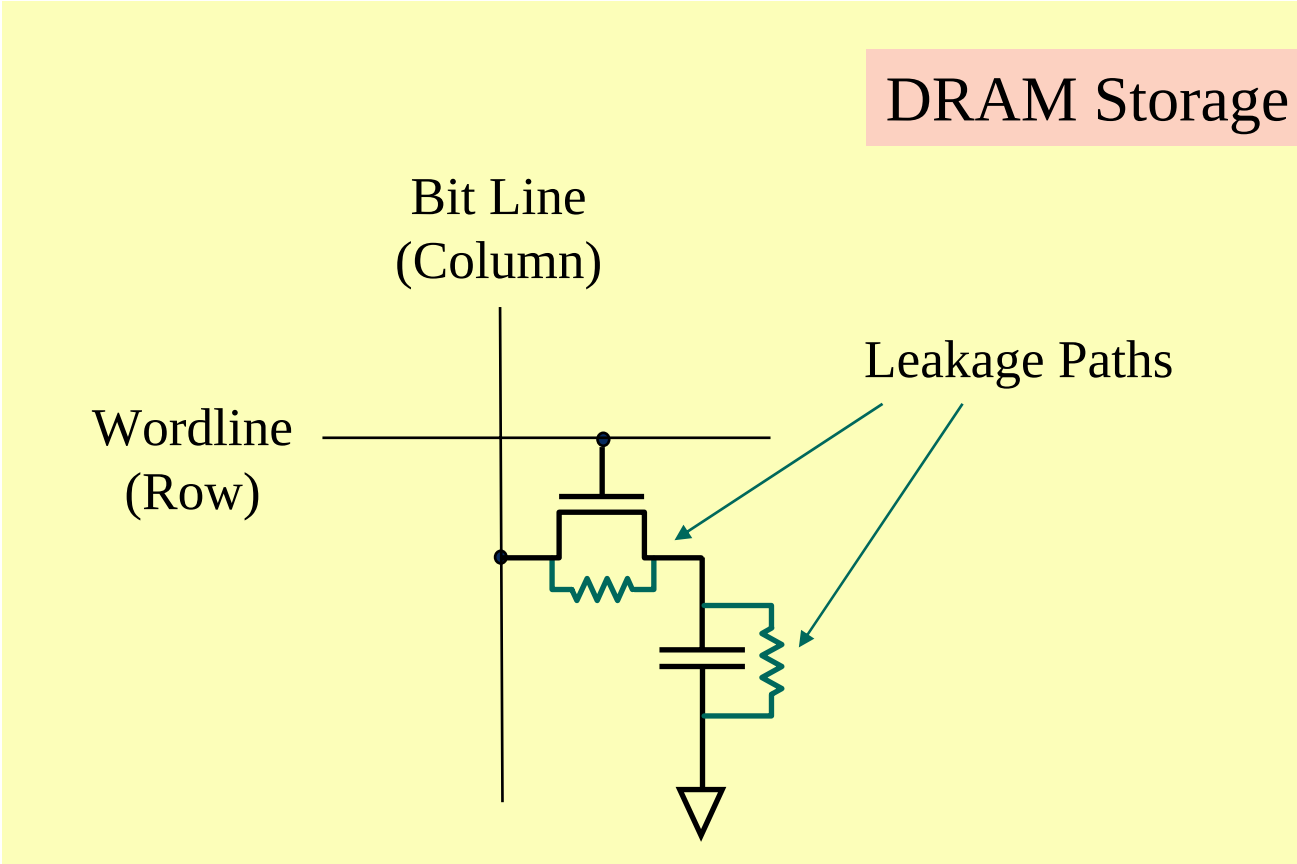


SDRAM Architecture



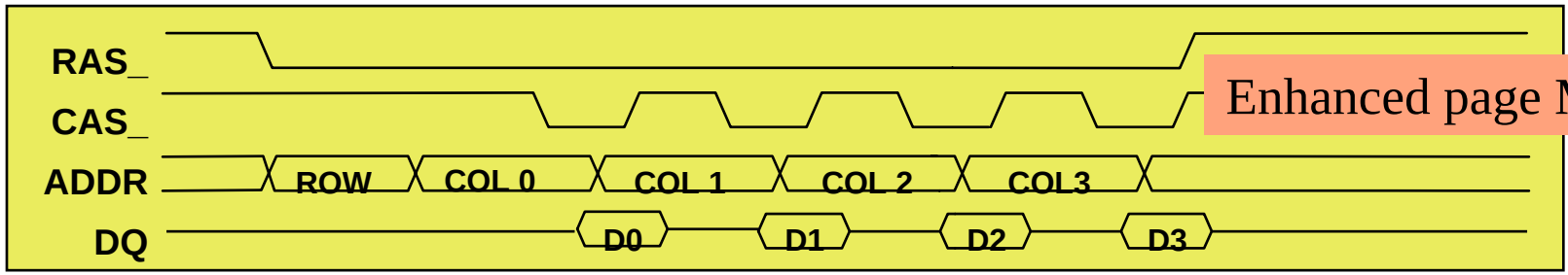


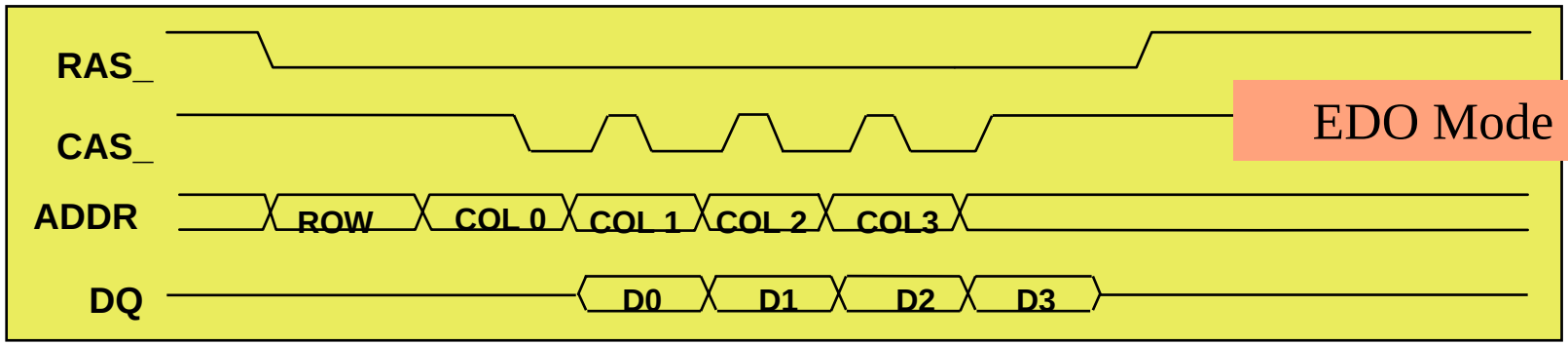
Why Refresh?

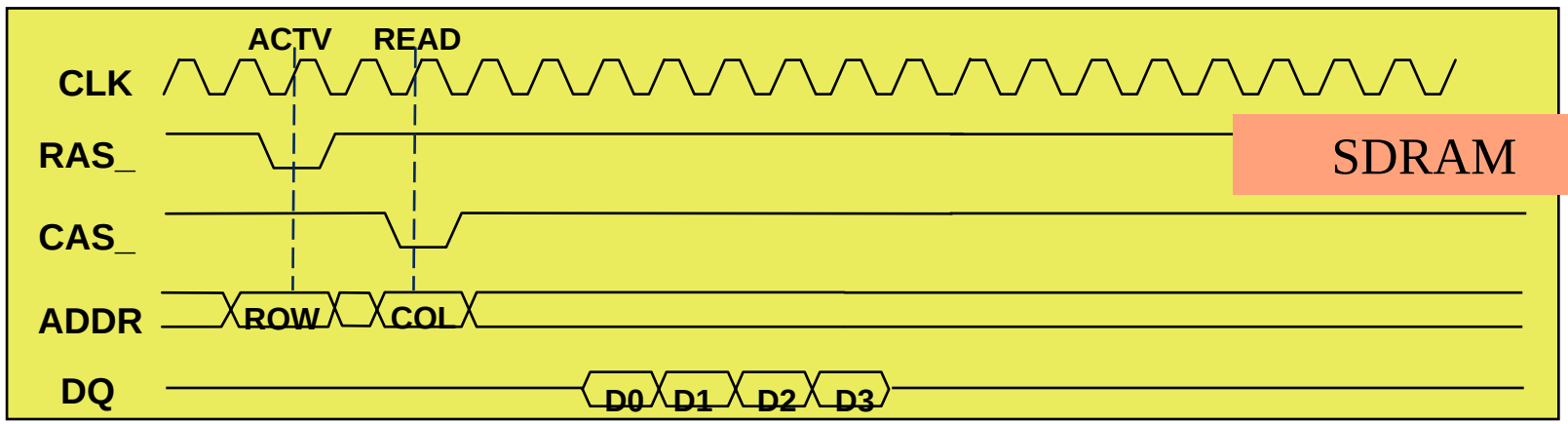


Charge leaks away over time. If nothing is done, in about a quarter of a second (200–300 milli-seconds), capacitors that were storing ones will be storing zeros!

Comparison of DRAM Timings

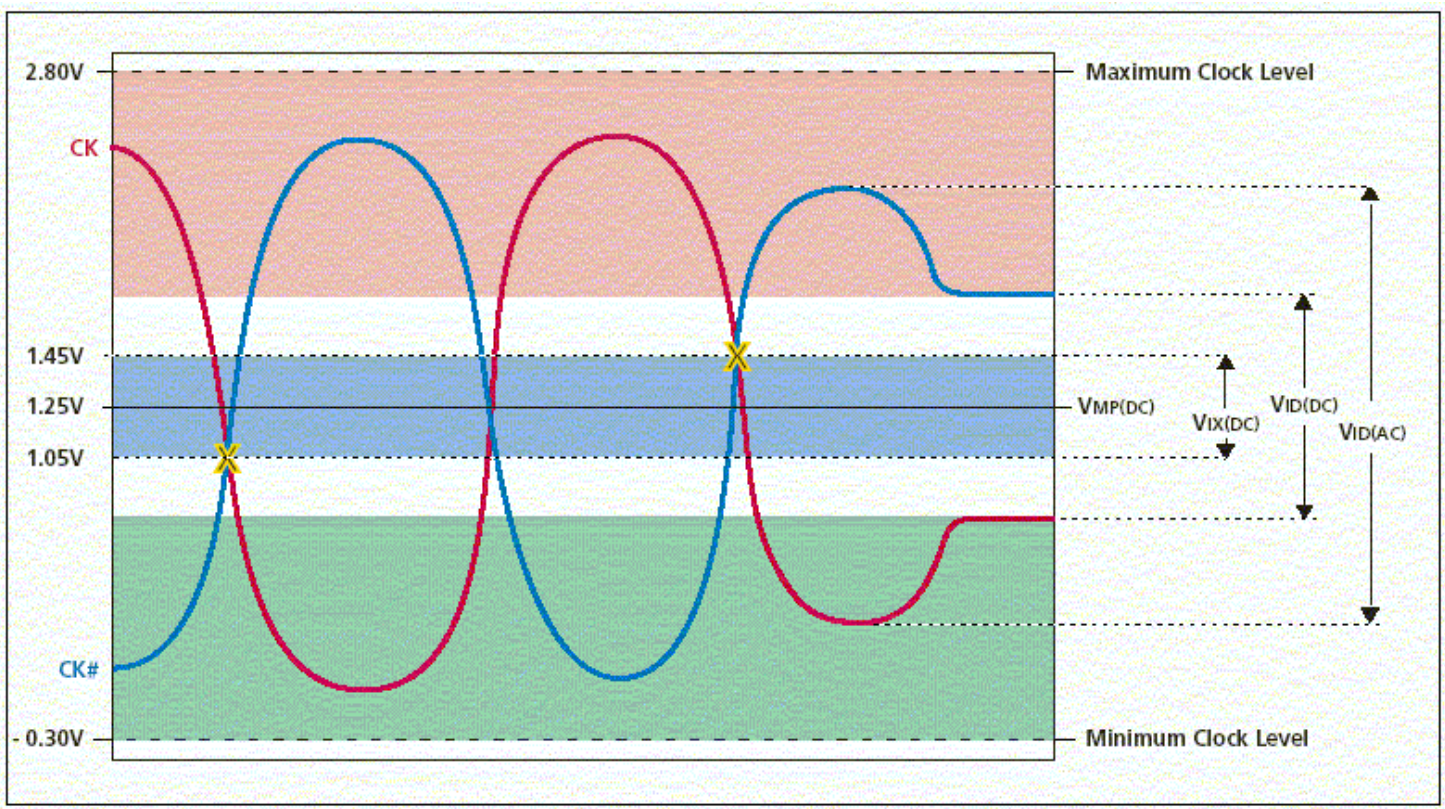






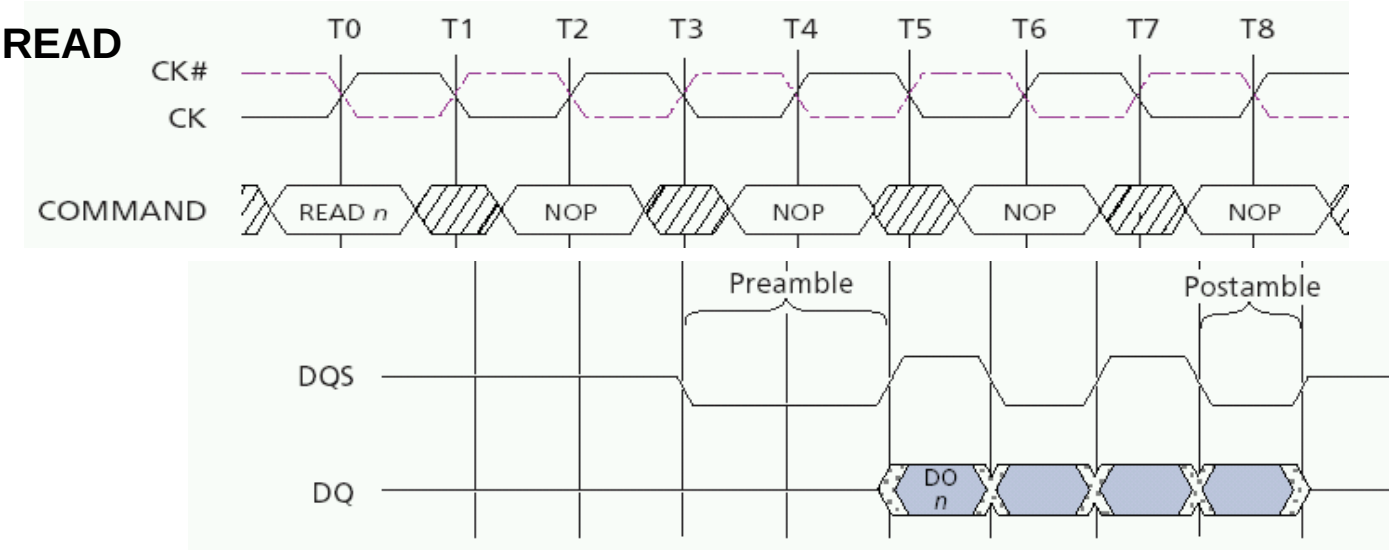
Basic DDR Differences from SDR

- Differential clock vs. single-ended clock
- Differential clock (crossing) more accurate than rising edge

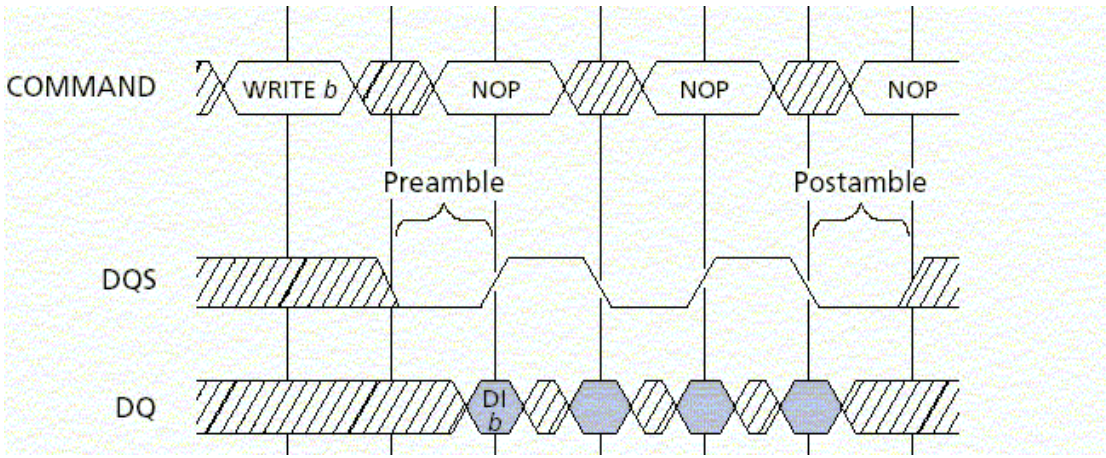


DDR DQS Strobe – READ/WRITE

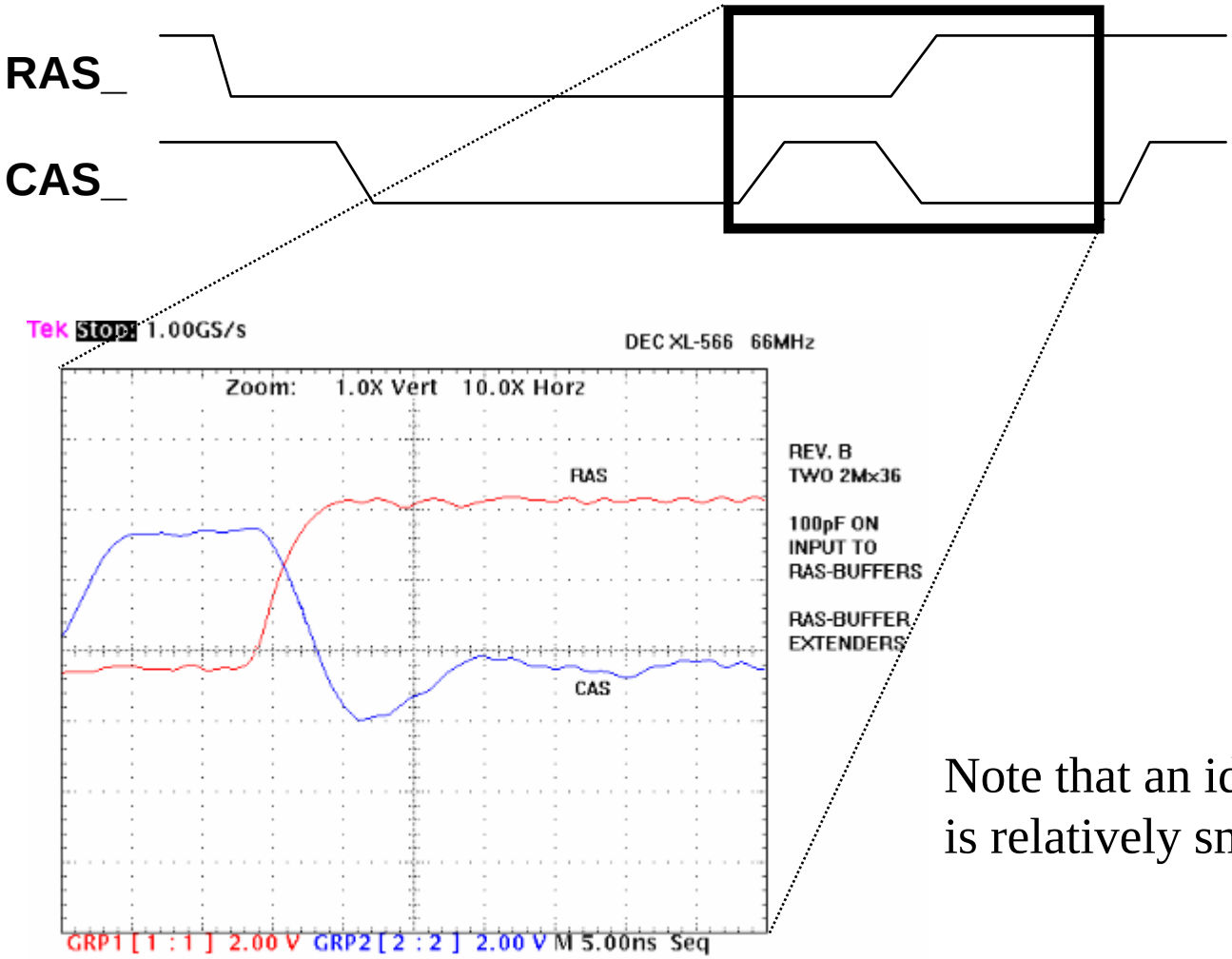
READ



WRITE



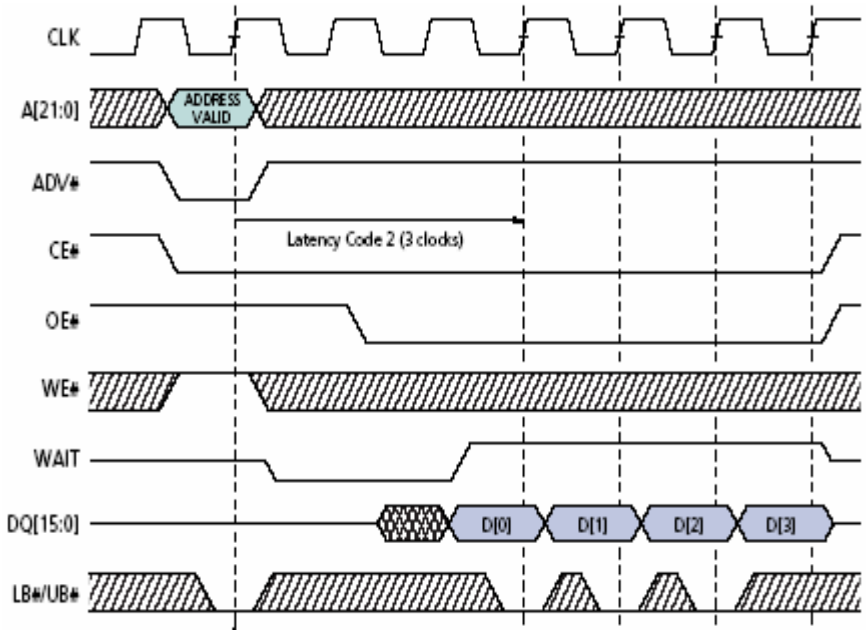
Ideal Signal Waveforms



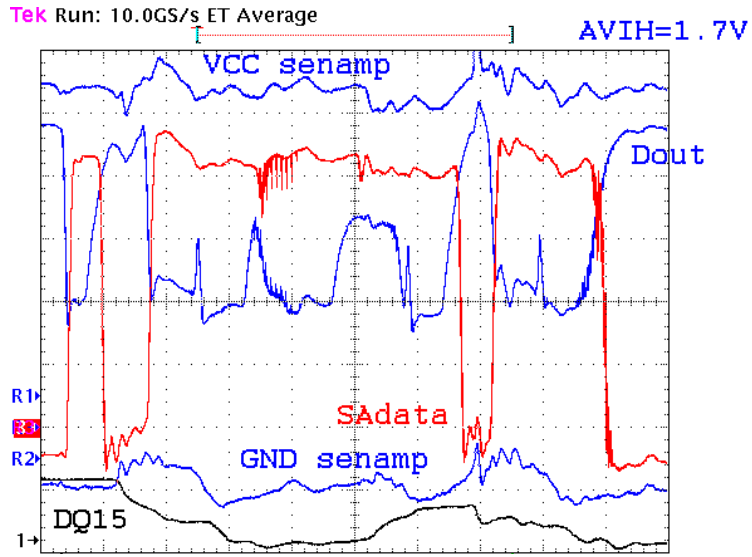
Note that an ideal signal is relatively smooth.

What is Real?

- Digital View



- Analog View



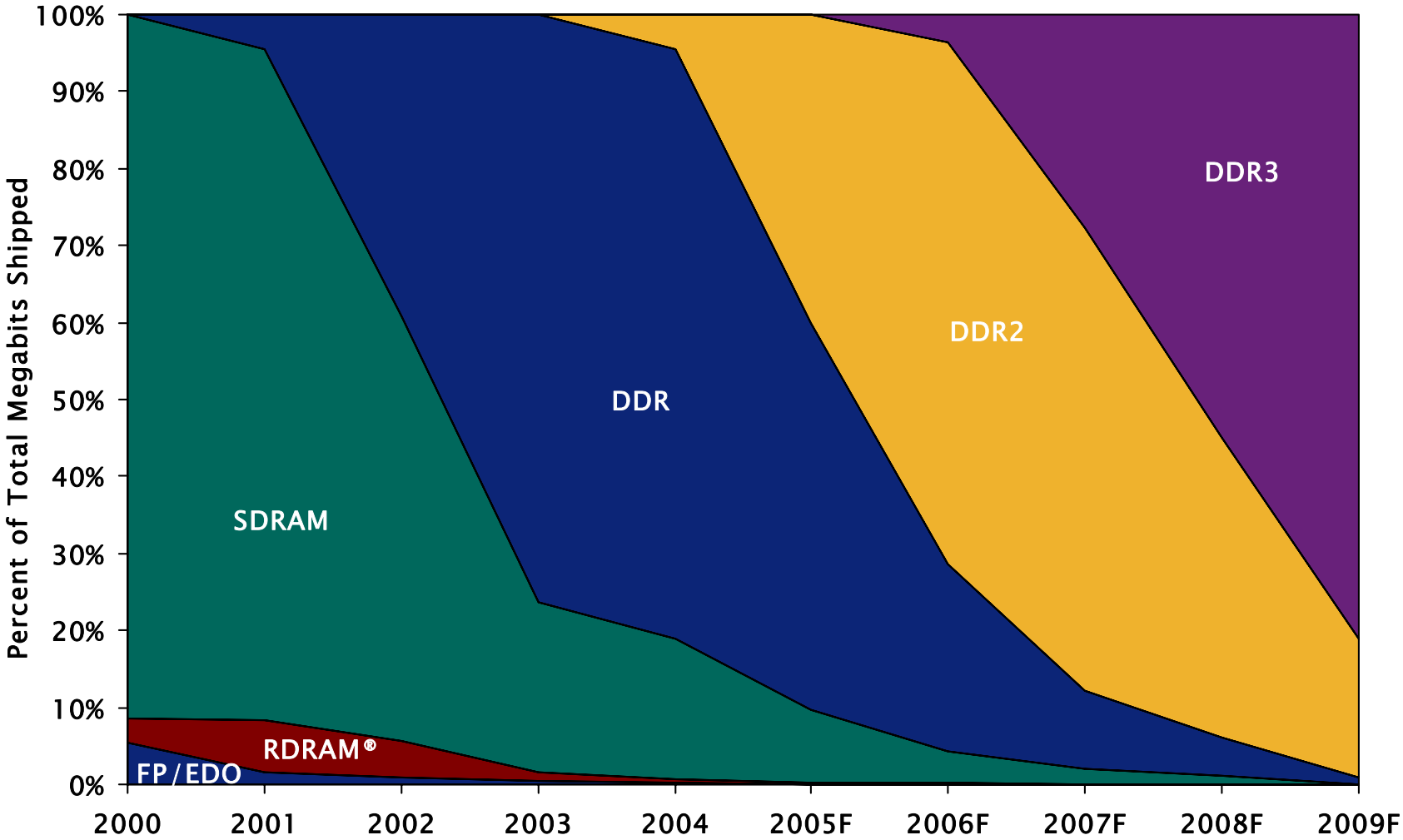
Basic DDR Differences from SDR

- Bi-directional data strobe (DQS) added to data bus
  - Why a data strobe?
    - Compensates for temperature, voltage, and loading
  - Strobe travels with data
    - During a WRITE to the DRAM, memory controller generates strobe
      - Strobe occurs at beginning of data valid
    - During a READ from the DRAM, the DRAM generates the strobe
      - Strobe occurs at midpoint of data valid

Major differences from DDR to DDR3

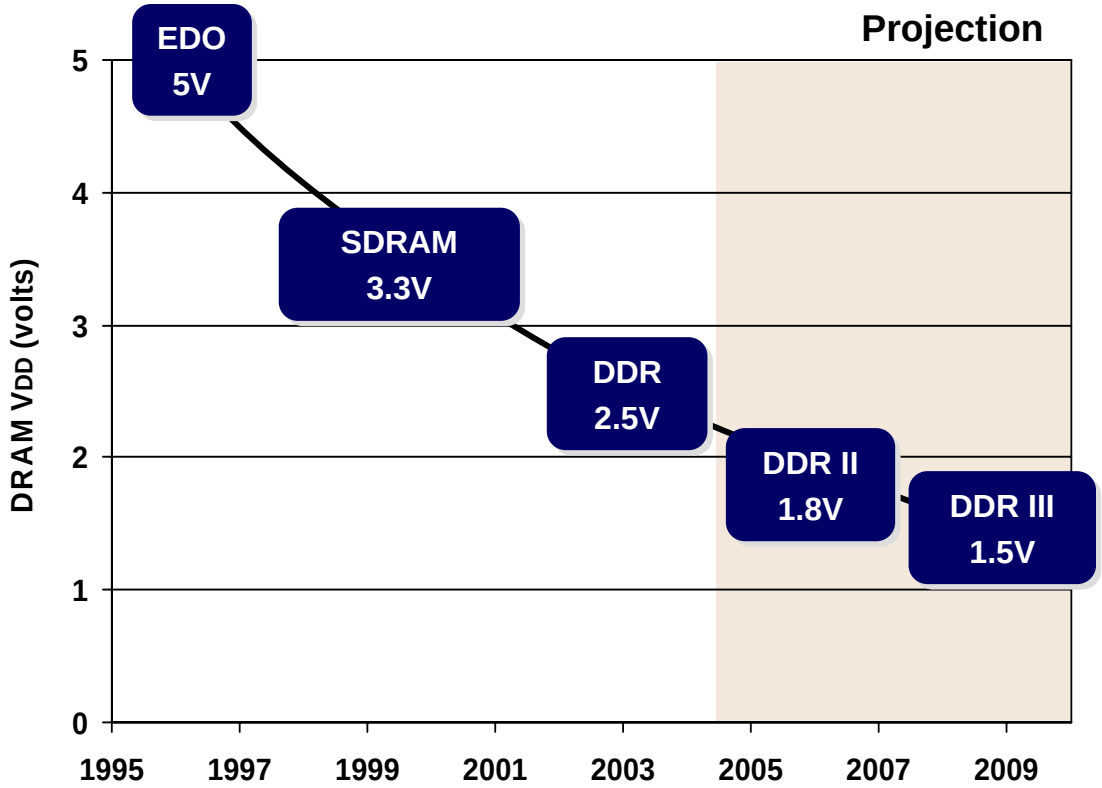
Feature/Option	DDR	DDR2	DDR3
Package	TSOP (66 pins)	FBGA only	FPGA 78-ball: x4, x8 FPGA 96-ball: x16
Voltage	2.5V 2.5V I/O	1.8V 1.8V I/O	1.5V
Densities	128Mb–1Gb	256Mb–2Gb	512Mb – 8Gb
Internal Banks	4	4 and 8	8
Prefetch *(MIN WRITE Burst)*	2	4	8
Speed (Data Pin)	200 MHz, 266 MHz, 333 MHz, and 400 MHz	400 MHz, 533 MHz, and 667 MHz	800, 1600 Mb/s
READ Latency	2, 2.5, 3 CLK	CL + AL CL = 3, 4, 5	CL + AL CL = 3, 4, 5
WRITE Latency	1 clock	READ latency – 1	AL + CWL CWL = 5,6,7,8

DRAM Technology Trends



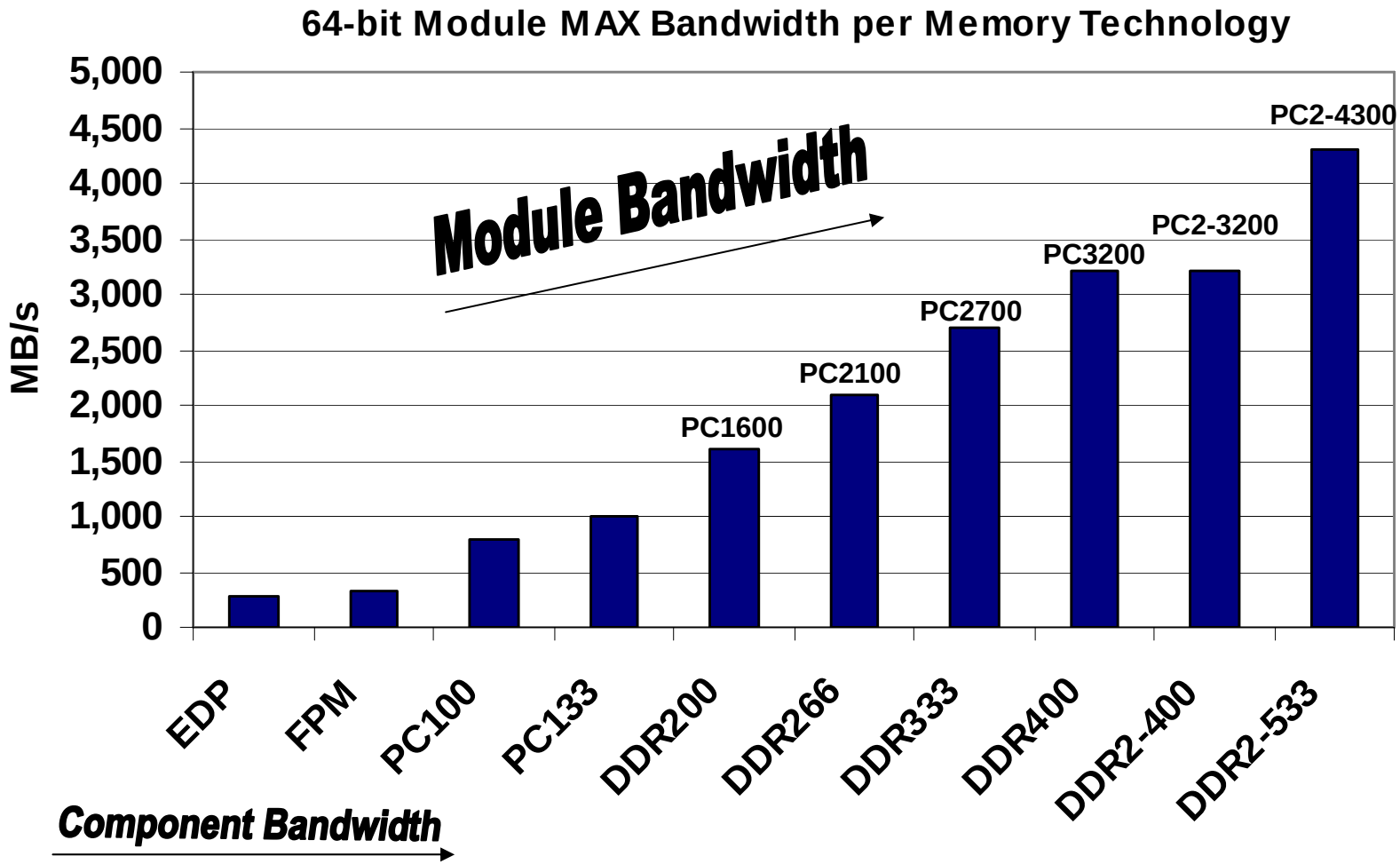
RDRAM is a registered trademark of Rambus Inc. Source: Micron market research, iSuppli 03/05

Main Memory Voltages

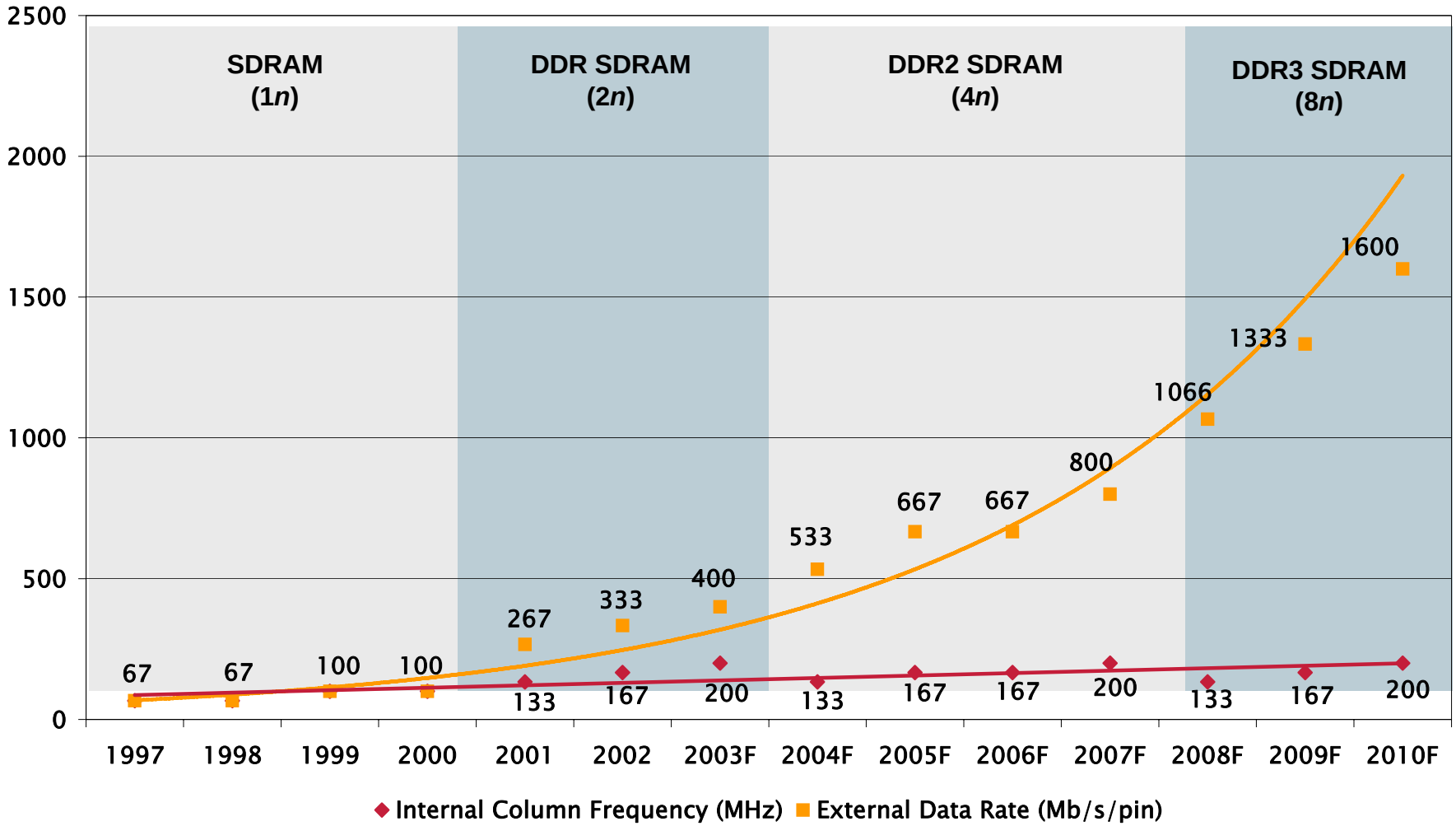


- VDD is being reduced with each new technology
- I/O voltages are also being reduced
- Each decrease of VDD allows significant power reductions

Performance – What Does This Mean?

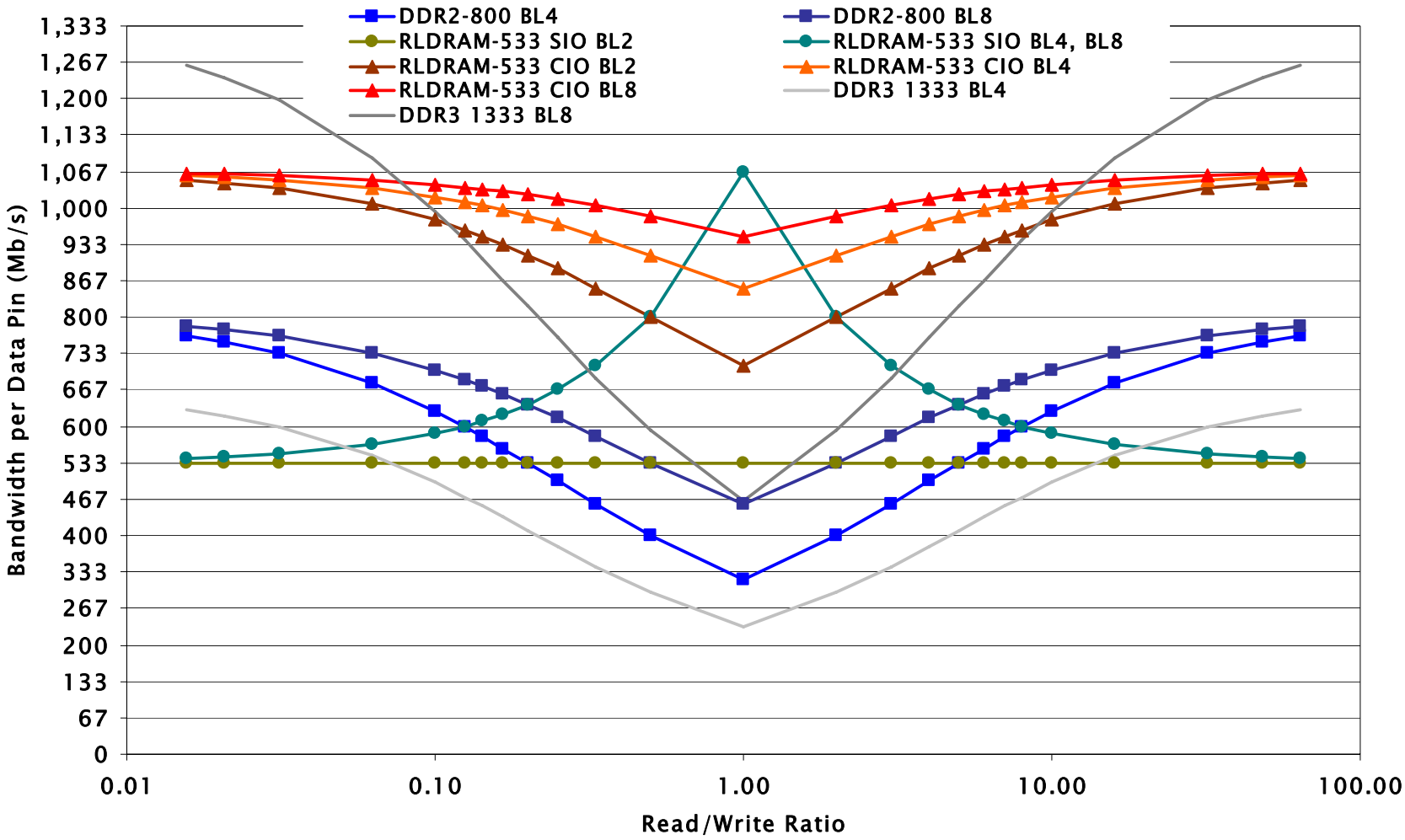


Increasing DRAM Internal Prefetch

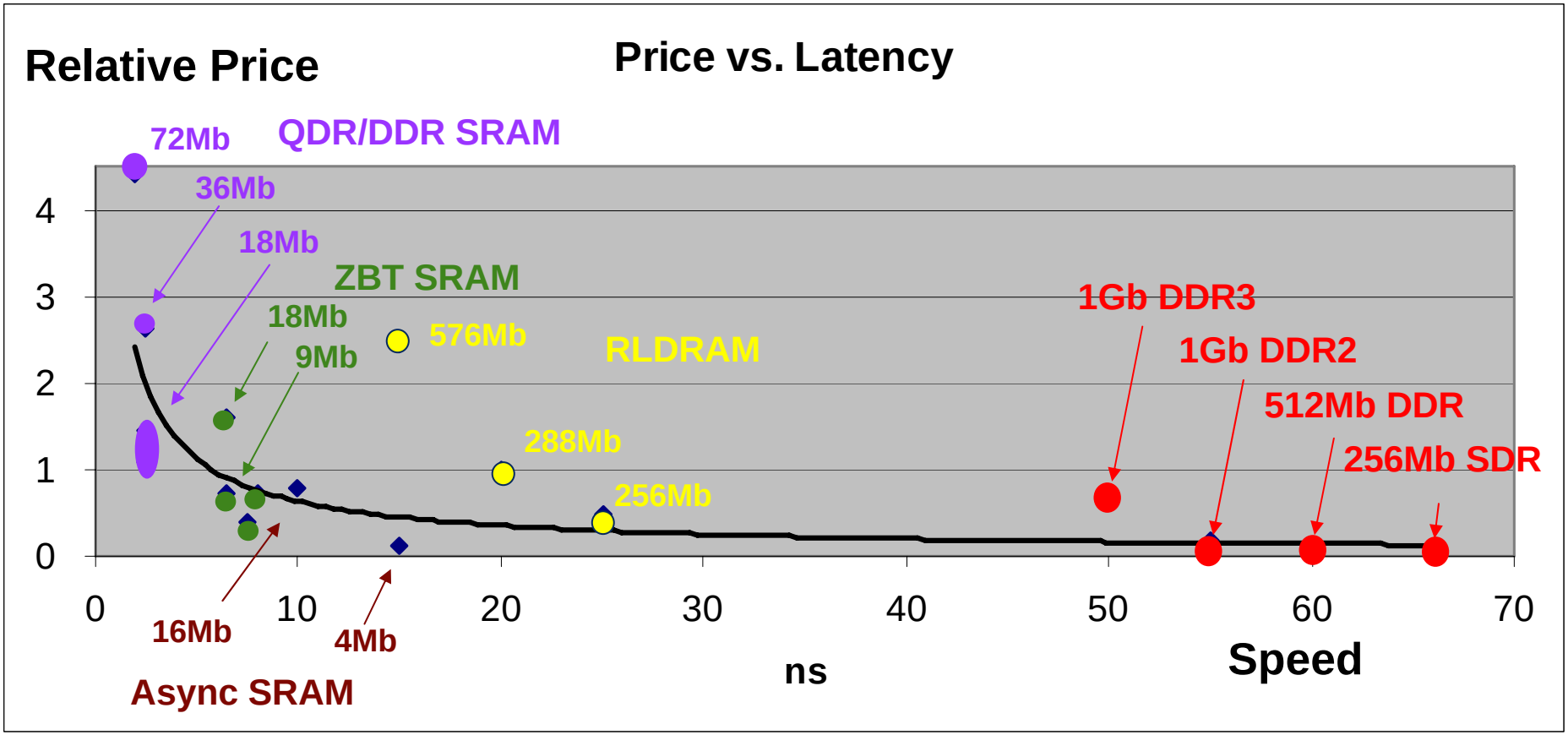


Source: Micron Marketing 09/03

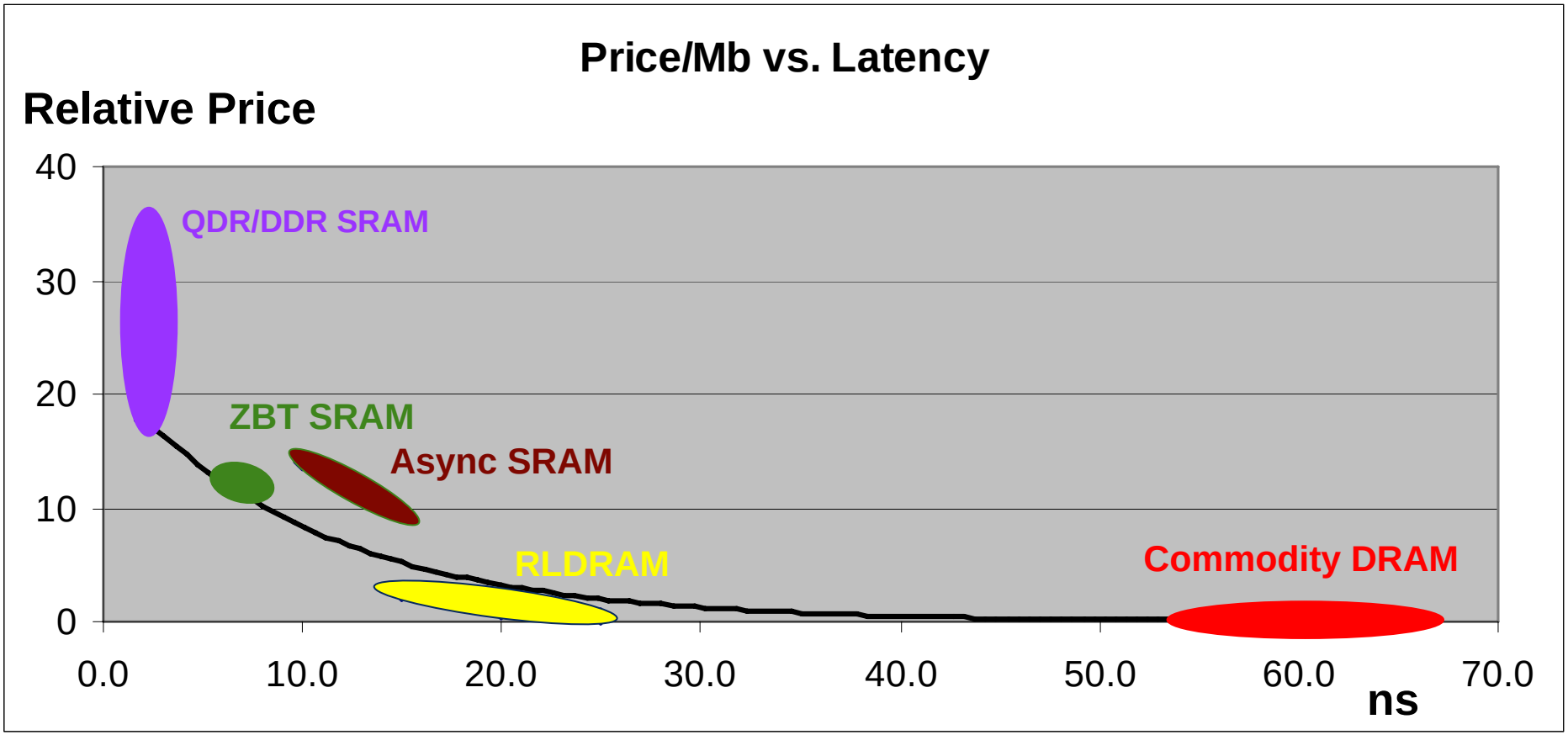
Maximum Bandwidth Comparison



Pricing Comparison by Technology



Technology Price/Mb Comparison



Low-Power, Mobile Solutions

Mobile Features
What Distinguishes it from Std SDRAM?

- Lower Power – Targets top four power issues (Supply and I/O Voltage, Self Refresh Current and Operating Current)
  - Typically 1.8V VDD and VDDQ option offered
  - TCSR – Temperature Compensated Self Refresh
  - PASR – Partial Array Self Refresh
  - Deep Power Down Feature
- Variable Drive Strength
- VFBGA Packaging – Smaller Form Factor

Mobile Features
Temperature Compensated Self Refresh

- First generation Mobile SDRAM designs allow manual setting of TCSR through the EMR (Extended Mode Register)
- All new (and some improved) designs incorporate an on-chip temperature sensor to dynamically control the self refresh rate automatically
- JEDEC LP-DDR specification had TCSR as optional – if an on-chip temp sensor is used, the EMR bits must be a "don't care" to allow backward compatibility

Mobile Features
Partial Array Self Refresh

- Ability to refrersh only one part of the total array. Programmed through the EMR (extended mode register)
- JEDEC LP-DDR specification had PASR as optional
  - Full array, 1/2 array, 1/4 array, 1/8 array, 1/16 array
- Difficult to use this feature in the real application; most of the customers currently are not using it due to their inability to track where the data they require is exactly
- Most customers do request this feature to allow for future upgrades from their side

Mobile Features
Deep Power Down

- JEDEC LP-DDR specification shows Deep Power Down as a design requirement
  - Device must be in all banks idle state prior to entering DPD
  - All memory data is lost
  - DRAM must be fully re-initialized to ensure proper functionality – LMR and EMR must be reloaded
- No customer usage currently known and no requests made to have this feature in future designs
  - Micron will continue to offer this feature to be fully JEDEC compliant

Mobile Features
Variable Output Drive Strength

- Offers customers the option to use a lower drive strength for lighter system loads or point-to-point environments
- Programmed through the EMR (extended mode register) – standard full and half drive settings
  - New series Mobile SDR/DDR SDRAM will include 1/4 and 1/8 drive setting in response to customer requests
- Customers are using this feature – especially for the SDR parts that exhibit higher full drive strength than they required

DDR Mobile SDRAM
How Does it Differ From Std DDR?

- **Design Differences**
  - DLL Omitted from Design
    - Reduces power consumption
    - Minimizes the DRAM's ability to run at higher frequencies
      - currently specified to 200MHz CL=3 and is pushing the limits of the design – customers pushing for tighter tAC specifications
  - No external VREF – internal to the DRAM design
  - Different initialization sequence required
  - Offered in x32 configuration
- **Main Specification Differences**
  - Lower IDD values – Operating current and Self Refresh
  - Some variations in timing
    - Minimum speed specified on Std DDR, LP-DDR can run at very slow speeds
    - Much higher tAC (access time from CK/CK#)
  - No DLL

Mobile Memory Comparison

	PSRAM	LP-SDR	LP-DDR	LP-DDR2 (S4)
MAX frequency	133 MHz	166 MHz CL = 3	200 MHz CL = 3	533 MHz CL = 8
Data rate (0% interleaving, 1:1 R/W, 1 Byte/access)	26.6 MB/s @ 133 MHz	16.6 MB/s @ 166 MHz	19.0 MB/s @ 200 MHz	16.7 MB/s @ 533 MHz
Data rate (25% interleaving, 1:1 R/W, 1Byte-32Byte/access)	168.5 MB/s @ 133 MHz	120.7 MB/s @ 166 MHz (x16) 177.3 MB/s @ 166 MHz (x32)	269.0 MB/s @ 200 MHz (x16) 318.9 MB/s @ 200 MHz (x32)	310.0 MB/s @ 533 MHz (x32)
Data rate (85% interleaving, 1:1 R/W, 32 Byte/access)	212.8 MB/sec @ 133 MHz	167.2 MB/s @ 166 MHz (x16) 316.7 MB/s @ 166 MHz (x32)	684.5 MB/s @ 200 MHz (x16) 1196.3 MB/s @ 200 MHz (x32)	2061.1 MB/s @ 533 MHz (x32)
Bus width (per device)	x16	x16, x32	x16, x32	x16, x32
Density	4-128Mb	64-512Mb	64Mb-1Gb	1-8Gb
Banks	1	4	4	8
VDD/VDDQ	1.8V/3.3V	1.8V/1.8V	1.8V/1.8V 1.8V/1.2V* 1.2V/1.2V*	1.8V/1.2V/1.2V/1.2V**
Package	54-ball VFBGA	54-ball VFBGA (x16) 90-ball VFBGA (x32)	60-ball VFBGA (x16) 90-ball VFBGA (x32) 152-ball VFBGA PoP*	TBD-JEDEC
Functional pin Count (MAX density, MAX width)	Std (128Mb): 47 AD MUX (64Mb): 31	(512Mb-x32): 57	(1Gb-x32): 62	(8Gb-x32***): 59
Burst options	4, 8, 16, 32*	1, 2, 4, 8 page	2, 4, 8, 16*	4, 8, 16

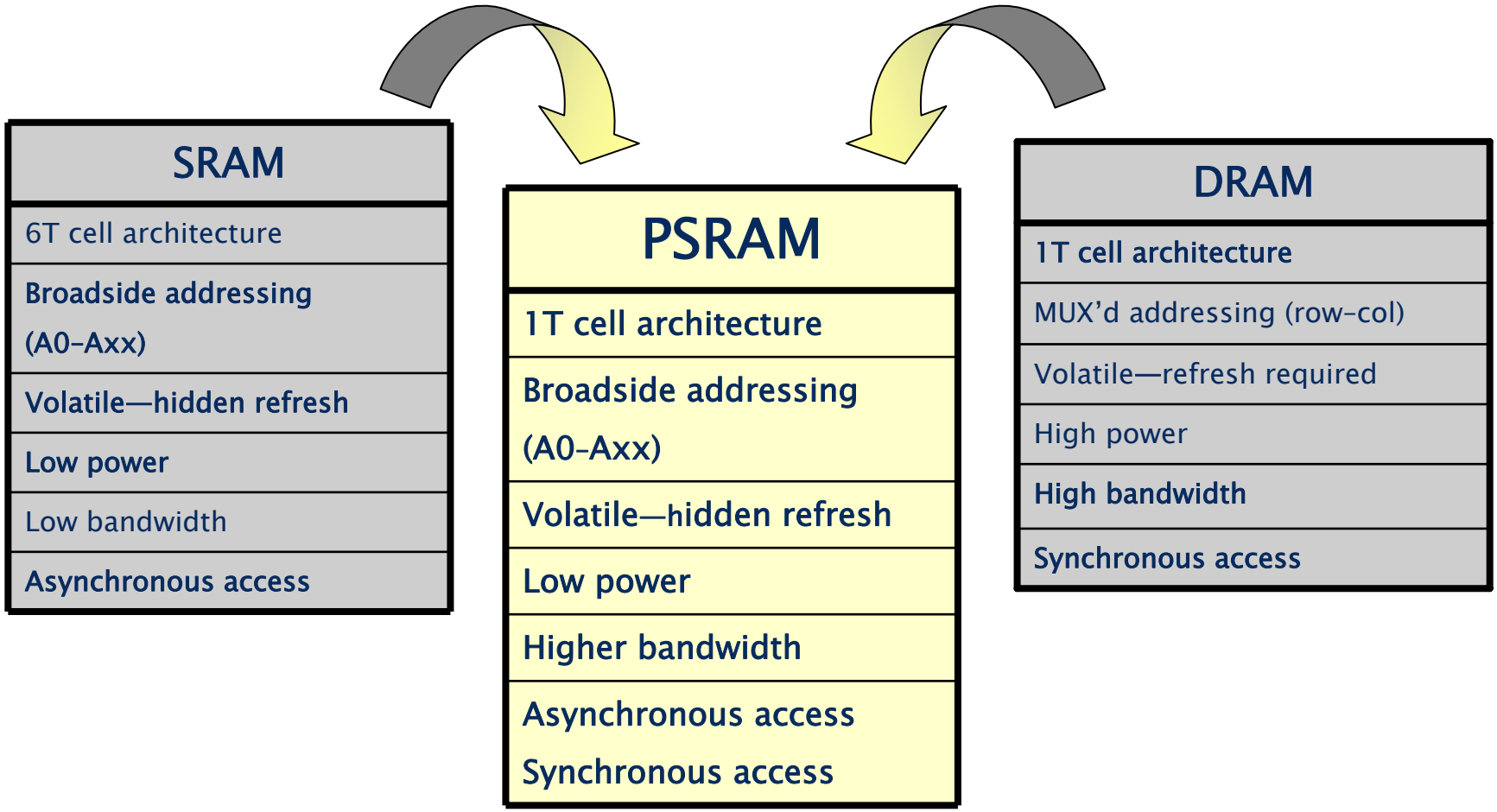
* Note: Not available for all densities; contact factory for availability

** Note: LP-DDR2 has four supplies: VDD1/VDD2/VDDCA/VDDIO

*** Note: Pin count does not change with density for LP-DDR2 due to muxed cmd/addr bus

What is a PSRAM?

- Psuedo-SRAM's name comes from its similarity to SRAM; however, internally PSRAM is a DRAM—combining the best of both products



Architectural Comparison

	CellularRAM® (PSRAM)	LP-SDRAM
Addressing	Broadside	Multiplexed
Refresh modes	Hidden	Auto/Self
Row size	2k	4k (128K device)
Interface optimized for?	Random access	Multibank access
Bank architecture	Single (1) bank	Multiple (4) banks
Density	4–128Mb	64–512Mb (SDR)
		64Mb–1Gb (DDR)
Voltage (Vcc/Vdd)	1.7–3.6V	1.8V
Voltage (Vccq/Vddq)	1.7–3.6V	1.8V

Why Use PSRAM instead of SRAM?

PSRAM can be used to replace sockets where SRAM has been traditionally used

Feature		Benefit
• Smaller die size (6T vs. 1T/2T)	→	• Lower cost part
• Increased density offering	→	• Ability to increase complexity and performance of end design
• Asynchronous interface	→	• Drop-in replacement
• Burst interface with variable latency	→	• Increased throughput and performance
• FBGA and TSOP* package	→	• Small footprint for mobile applications

* In design

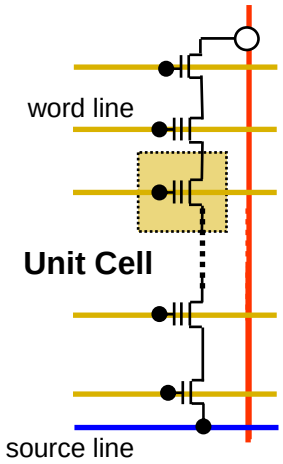
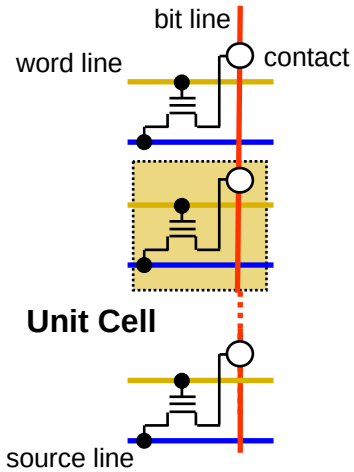
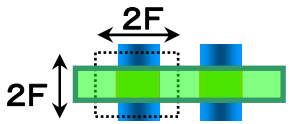
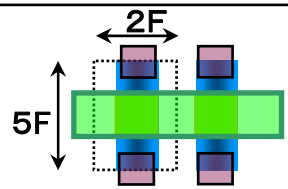
Nonvolatile Technologies

Micron

Nonvolatile Technologies
(Relative Comparison)

Technology	Fuse (OTP)	NOR	NAND	eMMC	MRAM	PCRAM
Power						
Density						
Speed read						
Speed write	NA					
Endurance			Requires block management			
Reliability			Requires ECC and block management			
Availability						Protos

Flash Memory Cell Comparison

	NAND	NOR
Cell array		
Layout		
Cross-section		
Cell size	$4F^2$	$10F^2$

- NAND Flash's small cell size enables high density and low cost

NAND vs. NOR: Basic Comparison

NAND

- Advantages
  - Fast writes
  - Fast erases
- Disadvantages
  - Slow random access
  - Byte writes difficult
- Applications
  - File (disk) applications
  - Any sequential data access
  - Shadow for embedded applications

NOR

- Advantages
  - Random access
  - Byte writes possible
- Disadvantages
  - Slow writes
  - Slow erase
- Applications
  - Replacement of EPROM
  - Execute directly from nonvolatile memory

NAND vs. NOR: Strengths and Weaknesses

Characteristic	NAND Flash (SLC) MT29F4G08A	NOR (Q-Flash®) MT28F128J3
Random access read	25µs (first byte) 25ns each for remaining 2,111 bytes	0.12µs
Sustained read speed (sector basis)	33 MB/s (x8)	20.5 MB/s (x8)
Random write speed	~220µs/2,112 bytes	180µs/32 bytes
Sustained write speed (sector basis)	19 MB/s	0.178 MB/s
Erase block size	128KB	128KB
Erase time per block (TYP)	2ms	750ms

NAND Flash is ideal for file storage, such as data or image files. If code is stored, it must be shadowed to RAM first (as in a PC).

NOR Flash is ideal for direct code execution (boot code).

MLC vs. SLC

	MLC	SLC
Features		
Bits per cell	2	1
Voltage	3.3V	3.3V, 1.8V
Data width (bits)	x8	x8, x16
Architecture		
Number of planes	2	1 or 2
Page size	2,112–4,314 bytes	2,112 bytes
Pages per block	128	64
Reliability		
NOP (partial page programming)	1	4
ECC (per 512 bytes)	4+	1
Endurance (ERASE/PROGRAM cycles)	~10K	~100K
Array Operations		
^{t}R (Max)	50µs	25µs
^{t}PROG (TYP)	600–900µs	200–300µs
^{t}BERS (TYP)	3ms	1.5–2ms
Relative price	1X	2X

Reliability of SLC is 10 times better!

Performance of SLC ~3 times better!

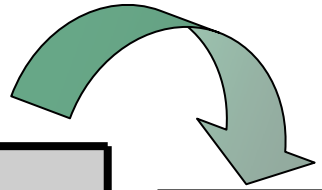
Cost premium is only about 2X

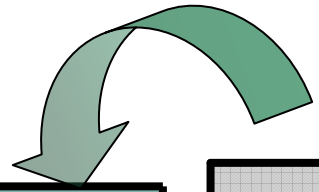
Another Option: eMMC (Managed NAND)

- The next logical step in the high-density NAND evolution for embedded applications
- Turns MLC NAND into a robust simple write/read memory
- Insulates the host from unnecessary details, including NAND block sizes, page sizes, planes, new features, process generation, MLC vs. SLC, wear leveling, and ECC requirements

What is Managed NAND (eMMC)?

- Managed NAND combines the advantages of MLC NAND with a controller, which address all of the complexities of MLC (ECC, wear leveling, and block management)
- Provides MLC densities at close to MLC prices



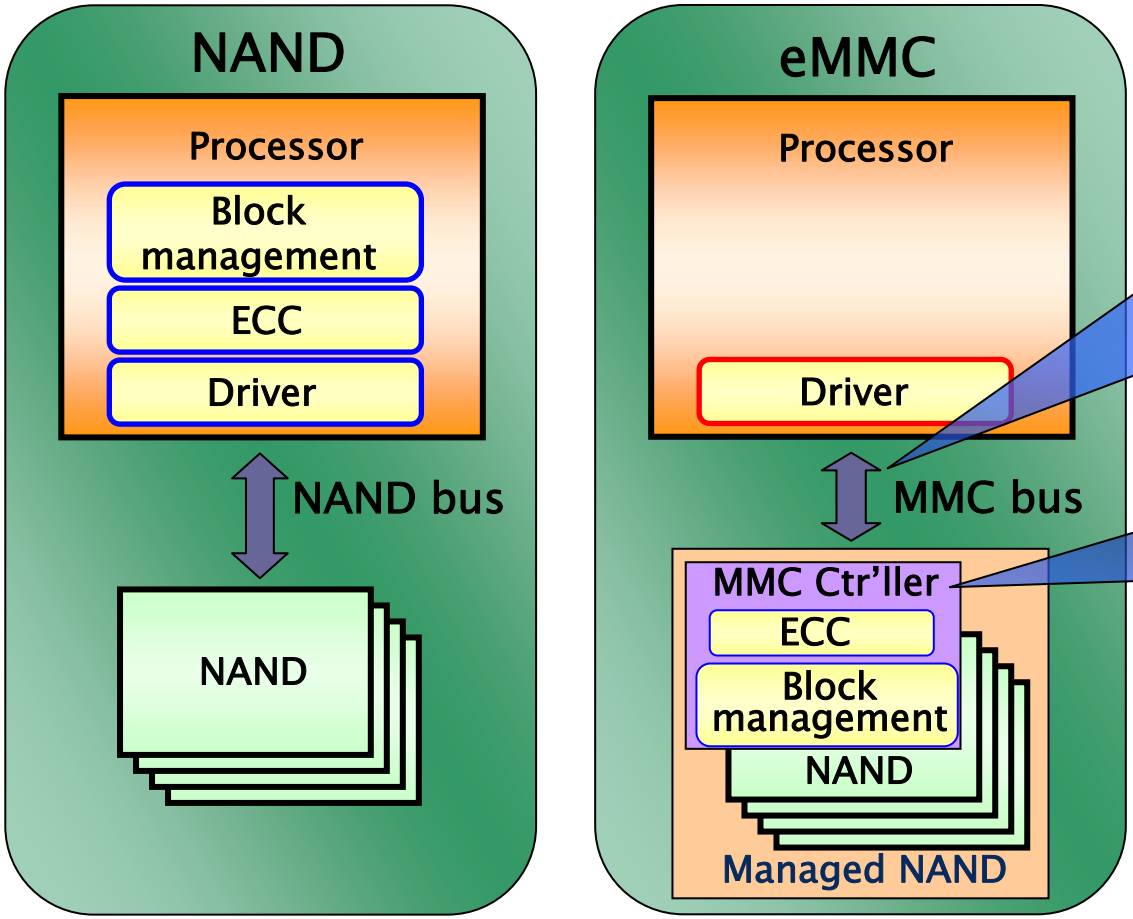


MLC NAND	
Advantages	Disadvantages
High density	Lower reliability (than SLC)
Lower cost (than SLC)	Lower performance

Managed NAND (eMMC)
Higher density (over SLC)
Improved cost (over SLC)
Improved reliability
Higher performance (over MLC)
Standard interface (MMC)
Single BGA package

Controller
Advanced ECC
Advanced wear leveling
Advanced block management
Advanced performance (dual channel)

What is eMMC (Managed NAND)



- Provides a consistent interface
- Published JEDEC /MMCA industry-standard interface

- Addresses the increased complexities of current and future MLC flash devices

Technology and vendor dependent

Technology and vendor independent

Summary


Micron®